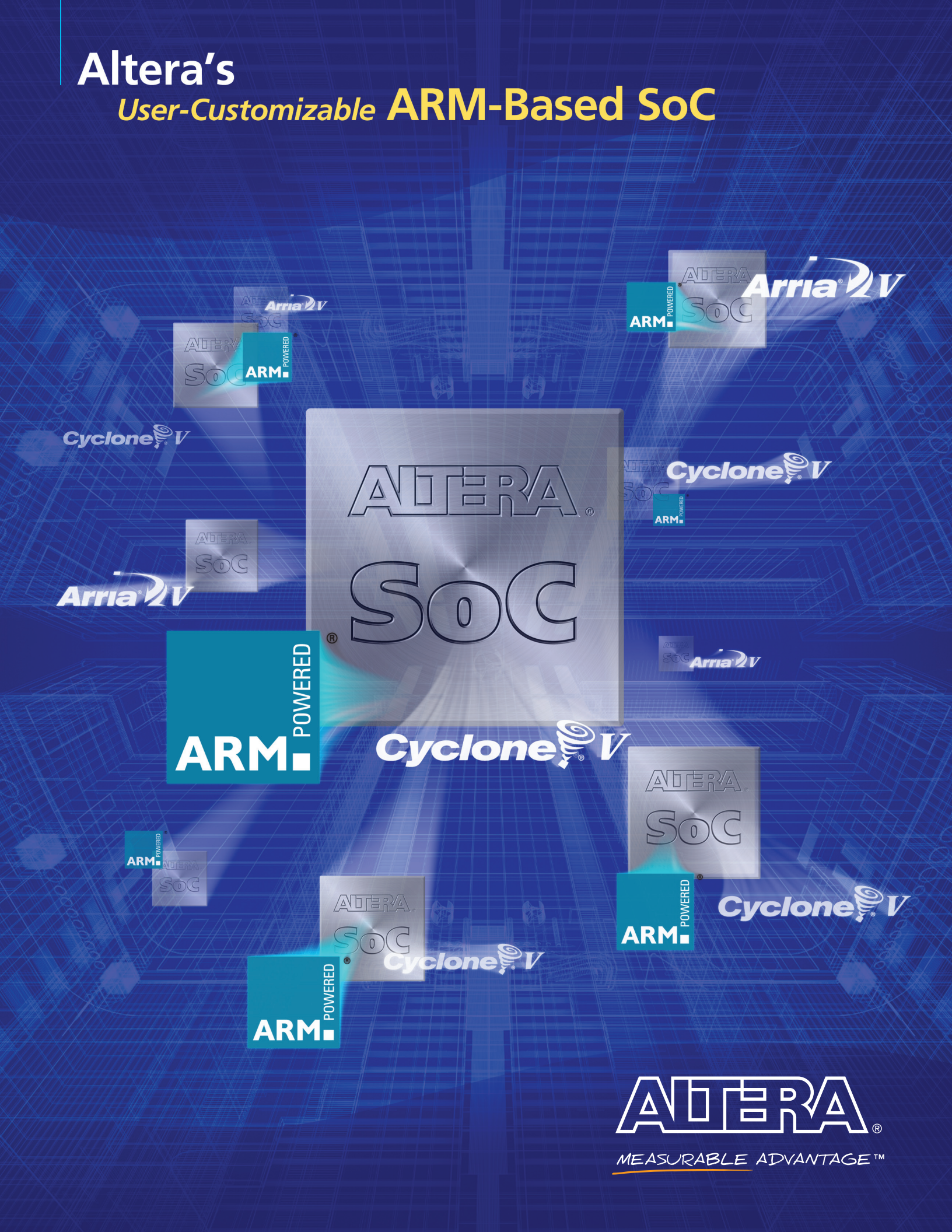
Altera's
User-Customizable ARM-Based SoC



Design the Way You Want

What if you could select the intellectual property (IP) and peripherals you need to quickly create a custom system on a chip (SoC) tailored to fit your application?

What if you could consolidate two discrete devices into one, reducing system power, cost, and board size while increasing performance?

What if you could use this chip to differentiate your end product in both hardware and software?

Now you can design that custom device with the Altera® SoC devices, members of our popular 28 nm Cyclone® V and Arria® V families. Our SoC devices help you keep up with changing market requirements and interface standards. We include a wide range of system peripherals, Altera IP, custom IP, and third-party IP that lets you quickly create a custom system using Altera design tools. For your software development needs, Altera and our partners provide comprehensive tools, operating systems, and middleware.

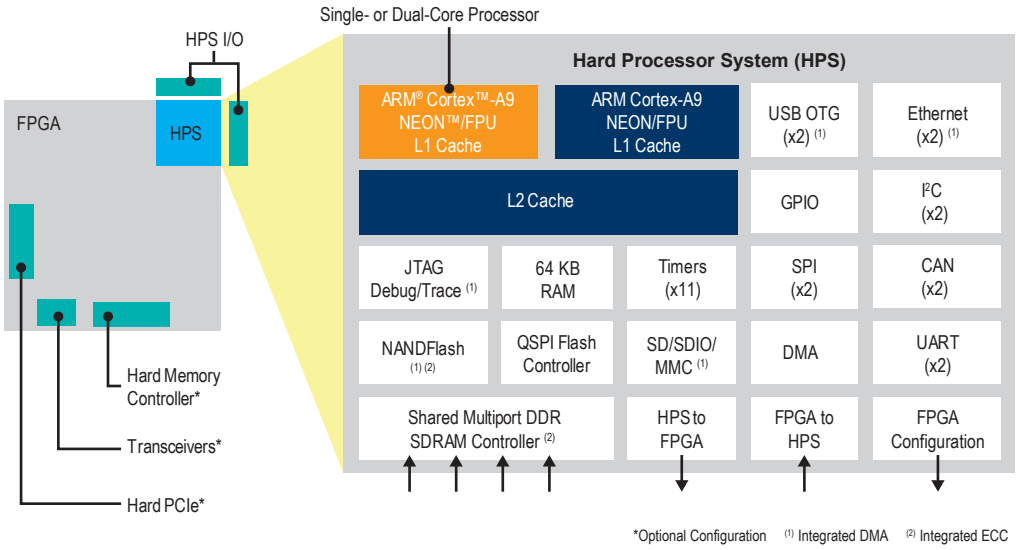
What Is an Altera SoC?

Our SoCs integrate an ARM-based hard processor system (HPS) consisting of a dual-core ARM® processor, peripherals, and memory controllers with the FPGA fabric using a high-bandwidth interconnect backbone.

The Altera SoC is ideal for:

- Reducing system power, cost, and board space by integrating two chips – the processor and FPGA – into one
- Improving system performance via high-throughput data paths between the HPS and the FPGA
- Differentiating your end product by customizing in both hardware and software
- Enhancing system reliability with built-in error correction code (ECC) and memory protection that protect your system against potential hardware or software errors
- Developing ARM-compatible software with unmatched target visibility, control, and productivity using Altera's exclusive FPGA-adaptive debugging

SoC Hard Processor System



ARM-Based Hard Processor System

The HPS consists of a dual-core ARM Cortex™-A9 MPCore™ processor, a rich set of peripherals, and a multiport memory controller shared with logic in the FPGA. The HPS gives you the flexibility of programmable logic combined with the performance and cost savings of hard IP.

- Embedded peripherals eliminate the need to implement these functions in programmable logic, leaving more FPGA resources for application-specific custom logic and reducing power consumption
- The hard multiport SDRAM memory controller, shared by the processor and FPGA logic, supports DDR2, DDR3, and LPDDR2 devices with an integrated ECC support for high reliability and safety-critical applications.

High-Speed Interconnect

High-throughput data paths between the HPS and FPGA fabric provide interconnect performance not possible in two-chip solutions. The tight integration between the HPS and FPGA fabric provides over 125 Gbps peak bandwidth with integrated data coherency between the processors and the FPGA.

Flexible FPGA Fabric

The flexibility offered by the FPGA logic fabric lets you differentiate your system by implementing custom IP or off-the-shelf preconfigured IP from Altera or its partners into your designs. This allows you to:

- Adapt quickly to varying or changing interface and protocol standards
- Add custom hardware in the FPGA to accelerate time-critical algorithms and create a compelling competitive edge
- Reduce power consumption and FPGA resource requirements by leveraging hard logic functions within the FPGA, including PCI Express® (PCIe®) ports and additional multiport memory controllers

SoCs: Extending the 28 nm FPGA Portfolio

Altera offers a full 28 nm device portfolio that is tailored to your design requirements. Our SoCs join this family of Cyclone V and Arria V FPGAs. You'll find dozens of devices that optimize requirements in areas such as performance, I/O resources, package size, power, and cost. What's more, you can take advantage of the 28 nm device families' common, productivity-enhancing design environment for faster design.

FPGAs for All Your Needs

Cyclone V FPGAs provide the industry's lowest system cost and power, along with performance levels that make the device family ideal for differentiating your high-volume applications. You get up to 40 percent lower total power versus the previous generation, efficient logic integration capabilities, and integrated transceiver options. You also get up to 150 GMACS and 100 GFLOPS digital signal processing (DSP) performance with our variable-precision DSP blocks. Cyclone V SoC devices offer a single- or dual-core Cortex-A9 processor, depending on your performance needs.

The Cyclone V family comes in six tailored options:

- Cyclone V E FPGA with logic only
- Cyclone V GX FPGA with 3.125 Gbps transceivers
- Cyclone V GT FPGA with 6.144 Gbps transceivers
- Cyclone V SE SoC with ARM-based HPS
- Cyclone V SX SoC with ARM-based HPS and 3.125 Gbps transceivers
- Cyclone V ST SoC with ARM-based HPS and 5 Gbps transceivers

Arria V FPGAs balance cost and power with performance for midrange applications such as remote radio heads, LTE base stations, and multifunction printers. You get high system performance due to a fast FPGA fabric, fast I/Os, and fast transceiver data rates. The DSP-rich Arria V FPGA fabric delivers up to 1,600 GMACS and 300 GFLOPS performance while helping you meet your cost and power requirements for applications in this space.

The Arria V family comes in four tailored options:

- Arria V GX FPGA with 6.5536 Gbps transceivers
- Arria V GT FPGA with up to 10.3125 Gbps transceivers
- Arria V SX SoC with ARM-based HPS and 6.5536 Gbps transceivers
- Arria V ST SoC with ARM-based HPS and up to 10.3125 Gbps transceivers

SoC Family

Family	KLE	Block Memory Bits (Mb)	Var. Prec. Multiplier Blocks	Max. FPGA User I/Os	HPS Dedicated I/Os	Max. Transceivers (GP)	Per-Transceiver Max. Data Rate (Gbps)	SoC Hard Memory Controller	FPGA Hard Memory Controllers	Hard PCIe
Cyclone V SoC	25	1.4	36	145	181	6	3	1	1	2 ea, Gen1
	40	2.7	58	145	181	6	3	1	1	2 ea, Gen1
	85	4.0	87	288	181	9	5	1	1	2 ea, Gen2
	110	5.6	112	288	181	9	5	1	1	2 ea, Gen2
Arria V SoC	350	17.3	809	528	208	30 / 16	6 / 10	1	3	2 ea, Gen2
	460	22.8	1,068	528	208	30 / 16	6 / 10	1	3	2 ea, Gen2

SoC Packages

		Non-Transceiver Devices (FPGA User I/Os)			Transceiver Devices (FPGA User I/Os, Transceivers)				
Family	KLE	U484-WB 19x19	U672-WB 23x23	F896-WB 31x31	U672-WB 23x23 (I/O, 3G/5G)	F896-WB 31x31 (I/O, 3G/5G)	F896-FC 31x31 (I/O, 6G, 10G)	F1152-FC 35x35 (I/O, 6G, 10G)	F1517-FC 40x40 (I/O, 6G, 10G)
Cyclone V SoC	25	66	145	–	145, 6	–	–	–	–
	40	66	145	–	145, 6	–	–	–	–
	85	66	145	288	145, 6	288, 9	–	–	–
	110	66	145	288	145, 6	288, 9	–	–	–
Arria V SoC	350	–	–	–	–	–	170, 12, 4	350, 18, 8	528, 30, 16
	460	–	–	–	–	–	170, 12, 4	350, 18, 8	528, 30, 16
HPS I/O		161	181	181	181	181	208	208	208

28 nm SoC Enhancements

Built on TSMC's 28 nm low power (28LP) process technology, the Cyclone V and Arria V SoC families provide low power consumption and feature significant architecture enhancements including:

- Efficient 8-input adaptive logic module (ALM)
- New 10 Kb (M10K) internal memory blocks
- New 640 bit memory logic array blocks (MLABs)
- Variable-precision DSP blocks
- Fractional phase-locked loops (PLLs) to reduce external oscillator needs
- Highly flexible clocking network
- Power-optimized MultiTrack routing architecture

Both families integrate an abundance of hard IP blocks. These hard IP blocks consume less power, ease your design process, and provide you with more logic resources for developing differentiated product features versus soft logic implementations and include:

- Hard memory controllers
- PCIe Gen2 with multifunction support

To protect your valuable IP investments, the SoCs provide additional design protection, including features such as 256 bit Advanced Encryption Standard with volatile and non-volatile keys.

Why Design with Our SoC?

You know that building a product with a strong architecture is key to ensuring that the final design meets your requirements. With Altera SoCs, you are already starting with a solid foundation that provides:

Increased System Performance

Our SoCs combine the performance and broad embedded software ecosystem of a dual-core ARM Cortex-A9 MPCore processor with the flexibility of Altera's FPGA fabric. Tight integration between the two provides system interconnect performance not possible in two-chip solutions: Higher bandwidth interconnect with a more than 125 Gbps processor (HPS)-to-FPGA interface and a high-bandwidth FPGA-to-SDRAM interface. Hardware acceleration with coherent memory access to all system masters in the FPGA and HPS accelerates critical sections of your code while keeping memory coherent.

Improved Reliability

We built in a variety of features to protect your system against potential hardware or software errors.

- ECC circuitry to make your system more robust and resilient against unexpected data errors or corrupted data
- CPU warm and cold reset initiates without affecting or reprogramming FPGA
- Shared DDR memory controller with an integrated protection unit keeps masters from accessing other memory regions

Increased Flexibility

Why should your design be constrained by your architecture? With our SoCs, you get the ability to optimize your design the way you want.

- Enables you to customize in both hardware and software
- Offers a variety of methods to boot the processor and configure the FPGA for more system design choices
- Dedicated hardened memory controllers in both the processor system and FPGA portion of the device save FPGA resources and guarantee timing closure
- Flexible product portfolio enables easy device migration (vertical and horizontal) with high-speed transceivers in all device densities

Lower System Cost

To help you lower your system cost, we have designed our SoCs so you can reduce design time and bill of materials (BOM) compared to multichip solutions.

- Integrates two or more chips into one (processor, DSP, FPGA) with a single-core option available
- Integrated PCI Express support runs across the entire device family
- Requires no power-off sequencing, eliminating need for external circuitry

Exclusive FPGA-Adaptive Debugging

The ARM Development Studio 5 (DS-5™) Altera Edition Toolkit dynamically adapts your custom configurations of the FPGA within the SoC to seamlessly extend embedded debugging capabilities across the CPU-FPGA boundary. The toolkit delivers an unprecedented level of debugging visibility and control that leads to substantial productivity gains.

- On-silicon debugging infrastructure combines with industry-standard ARM DS-5 tool to offer the best from both worlds—intuitive, easy-to-use debugging interface and Altera-exclusive FPGA-adaptive debugging capabilities
- True multicore debugging capabilities, whole-chip visibility and control, and automatic FPGA register view
- Premium JTAG-based debugging capabilities including cross triggering, trace, and correlation of CPU and FPGA events
- gdbserver compatibility enables Linux application debugging

Designing for the Future

Whatever direction you take your future designs, we'll be there to help. Our device portfolio and roadmap include high-end, midrange and low-end applications, built on leading-edge process technologies from TSMC (28 nm and 20 nm) and Intel Corporation (14 nm Tri-Gate). We offer forward migration of software for future devices to protect your software investment. Our average product cycle is 15 years, with many of our products having lifetimes in excess of 20 years, so you can design in our products with confidence.

Where You Can Use Our SoCs

We understand the requirements of end market solutions that drive silicon and IP development. That's why we optimized our SoCs for real-world applications. Example applications ideally suited for Cyclone V and Arria V SoCs:

Applications for SoC by Device

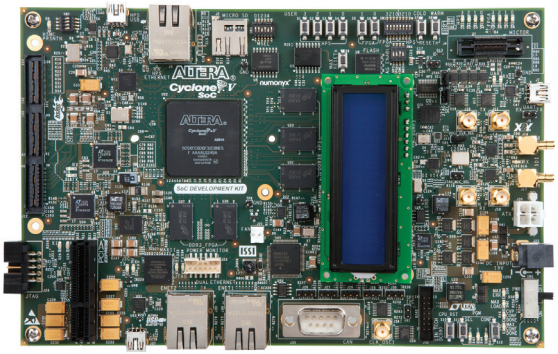
Industry	Target Applications	Key Functions	Cyclone V SoC				Arria V SoC	
			25	40	85	110	350	460
Factory Automation	Industrial I/O	Sensor interfaces, safety	•	•	–	–	–	–
	Industrial networking	Industrial communication/network protocol bridging, safety	•	•	•	•	–	–
	Programmable logic controllers (PLCs)/human machine interface (HMI), drives, servos	Control loop, energy-efficient inverter, communication protocols, I/O, safety	•	•	•	•	–	–
Smart Energy	Renewable energy, transmission and distribution, secure communication	Inverter, power management, protection relays, communication standards, security, and safety	•	•	•	•	–	–
Video Surveillance	IP camera	Wide dynamic range (WDR) camera, high-definition (HD)video, advanced video analytics	–	–	•	•	•	–
Automotive	Advanced driver assistance, infotainment	Video processing, video analytics, communication	•	•	•	–	–	–
Wireless Infrastructure	Remote radio unit, LTE mobile backhaul	Signal processing, baseband processing	–	–	–	•	•	•
Wireline Communications	Router, access, Edge equipment	Routing protocols, link management, OAM	–	–	–	•	•	•
Broadcast	Studio, video conferencing, professional audio/visual (A/V)	Audio and video CODEC, video over IP, PCIe capture, video and image processing	–	–	–	•	•	•
Defense & Aerospace	Night vision, secure communications	Video and image processing	•	•			•	•
	Intelligence, instrumentation	Data processing, control and deep packet inspection	–	–	–	•	•	•
Medical	Diagnostic imaging, instrumentation	Ultrasound imaging, signal processing	–	–	–	•	•	•
Compute and Storage	Multifunction printer, chassis management	Scan and print algorithms, temperature voltage monitoring/remote access	–	–	•	•	•	•

Cyclone V SoC Development Kit

The Altera Cyclone V SoC Development Kit offers a development platform to rapidly create custom ARM processor-based SoC designs. The kit includes a Cyclone V SoC development board and the Altera SoC Embedded Design Suite featuring the ARM Development Studio 5 (DS-5) Altera Edition Toolkit.

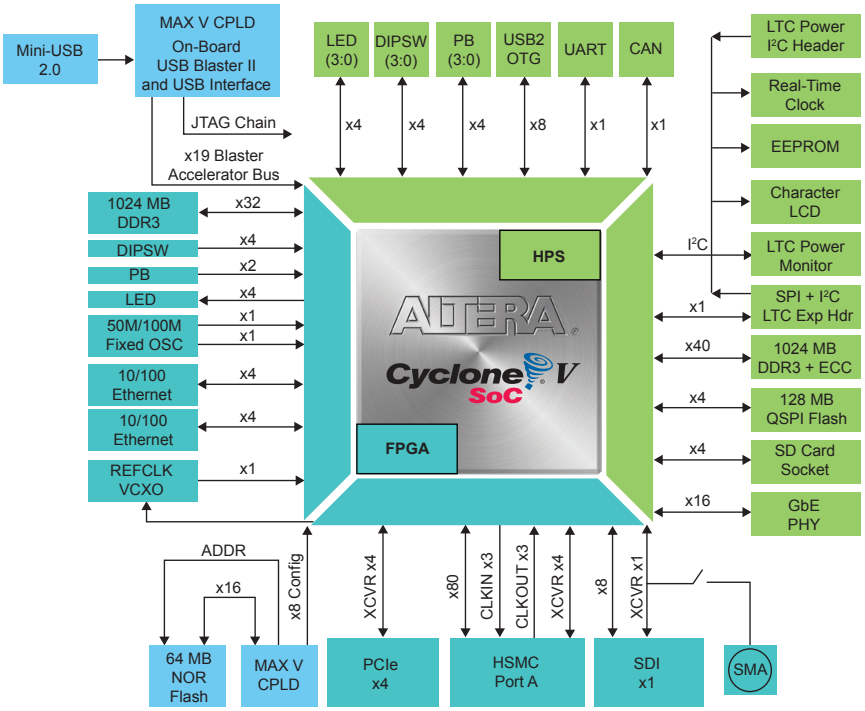
The development board includes the following features and interfaces:

- Cyclone V SX SoC - 800 MHz, 110K LE
- 2 GB DDR3 SDRAM (1 GB processor and 1 GB FPGA)
- Ethernet, USB 2.0 On-The-Go (OTG), CAN, I²C, and UART interfaces
- Integrated USB-Blaster™ II circuitry
- PCIe (rootport and endpoint support)
- Power supply and all cables
- Boots Linux on power up
- Expansion header (HSMC) *



*Application-specific daughtercards, available separately, support a wide range of I/O and interface standards.

Board Block Diagram



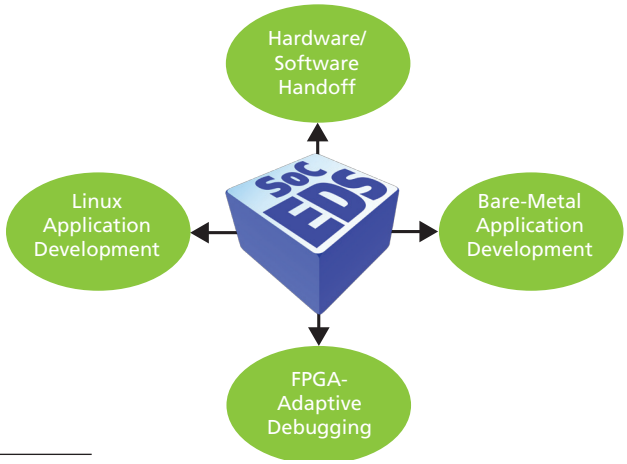
For more details on the Cyclone V SoC Development Kit, pricing, or ordering information, visit www.altera.com. or contact your local Altera sales representative.

Jump Start Software Development

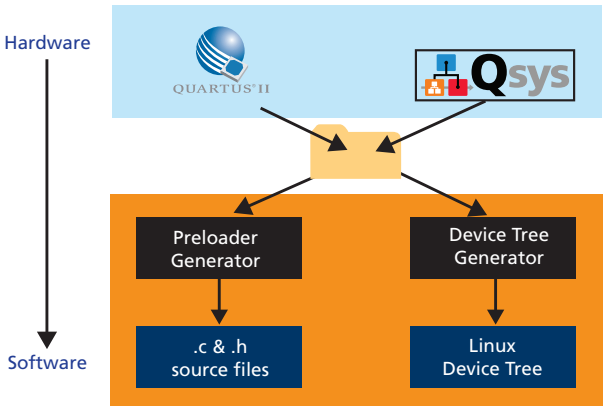
In any embedded system development project, software design typically takes up the bulk of time and resources. With the Altera SoC Embedded Design Suite (EDS), you get all the tools you need to work more productively, improve your software quality, and ultimately get to market faster.

The SoC EDS is a comprehensive tool suite for embedded software development on Altera SoC devices. It contains development tools, utility programs, run-time software, and application examples to jump start firmware and application software development.

Altera SoC Embedded Design Suite



Hardware-to-Software Handoff Utility Tools



Hardware-to-Software Handoff

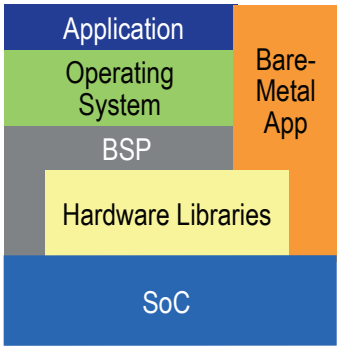
As part of the SoC EDS, the hardware-to-software handoff utilities allow FPGA and software design teams to work independently and follow their familiar design flows. These utilities take the Altera Quartus® II and Qsys output files and generate handoff files for the software design flow. As software engineers steer clear of FPGA development, they can focus on software design and be more productive.

Linux Application Development

SoC EDS includes U-Boot and Linux build environments, source files, and pre-built binaries. For Altera SoC development boards, these binaries can be run right out-of-the-box to jump start software development.

Our Linux build environment is based on the Yocto project for an open, versatile, and cost-effective solution for developers. Yocto, an open-source collaboration project, provides templates, tools, and methods to help developers create custom Linux-based embedded systems faster and easier Our SoC EDS also allows for easy transition to commercial embedded Linux distributions as most major vendors have adopted Yocto.

Hardware Libraries Abstract SoC Hardware



Firmware Development

The SoC EDS' embedded application binary interface (EABI) GNU compiler tool chain and SoC hardware libraries support bare-metal usage such as board bring-up support, device driver development, and optimized hardware access.

The SoC hardware libraries provide a low-level software interface to the underlying SoC hardware implementation. This application programming interface (API) provides easy access, configuration, and control of SoC hardware resources.

Availability

The SoC EDS is available in two editions: Subscription Edition and the free Web Edition. Designed for firmware and bare-metal developers, Subscription Edition enables full FPGA-adaptive debugging via an Altera USB-Blaster II connection. For Linux software developers, the free Web Edition allows application development over an Ethernet connection.

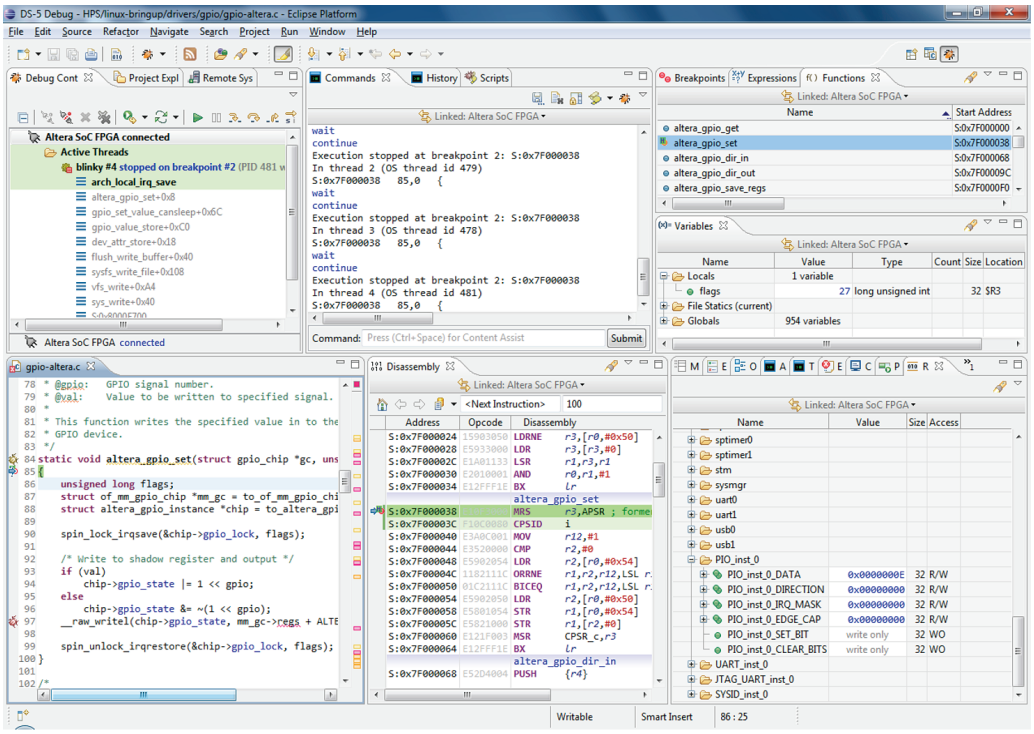
SoC EDS Editions

	Web Edition	Subscription Edition
Board Bring-up		Yes
Device Driver Development		Yes
Operating System Porting		Yes
Bare-Metal Programming		Yes
Linux Application Development	Yes	Yes
Multicore Debugging		Yes
System Debugging		Yes

FPGA-Adaptive Debugging

At the heart of the SoC EDS is the ARM Development Studio 5 (DS-5) Altera Edition Toolkit. By combining the ARM DS-5 advanced multicore debugging capabilities with FPGA-adaptivity and a seamless link to the Altera's SignalTap™ II logic analyzer, the toolkit provides you with an unprecedented level of full-chip visibility and control.

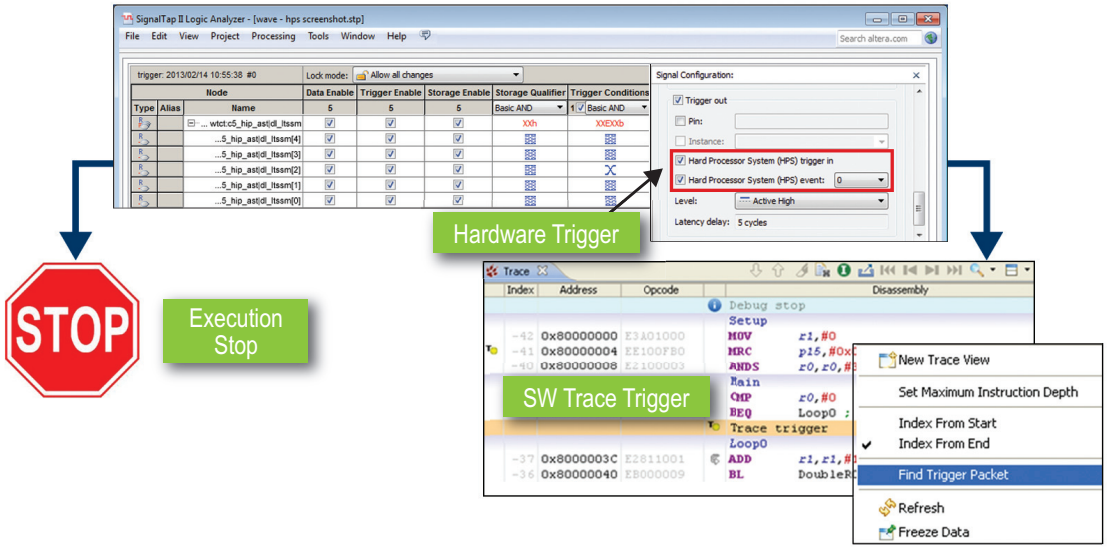
ARM DS-5 Altera Edition Toolkit



The toolkit displays pre-configured CPU subsystem peripheral register views and enables automatic generation of register views for peripherals in the FPGA fabric. All register views are self-documenting and organized by peripherals, registers, and bit fields.

Working with the Altera SignalTap II Logic Analyzer, the toolkit provides advanced, signal-level hardware cross- triggering between the CPU and FPGA domains. Using this capability, software and FPGA designers can analyze the captured trace and co-debug across the hardware-to-software boundary.

Cross-Triggering Between CPU and FPGA Domains



With the ARM DS-5 Altera Edition toolkit, you can efficiently debug code running on the dual-core CPU subsystem as well as IP synthesized into the on-chip SoC's FPGA fabric for higher productivity, better software quality, and faster time to market.

Key features include:

- Support for board bring-up, driver development, operating system (OS) porting, bare-metal, and Linux application development
- Development and debugging support for systems running in symmetric multiprocessing (SMP) and asymmetric multiprocessing (AMP) modes
- Simultaneous debug and trace connection for ARM Cortex-A9 processors as well as any custom cores with ARM CoreSight™ trace macrocells synthesized on the FPGA fabric
- Allows non-intrusive capture and visualization of signal events in the FPGA fabric, time- correlated with software events and processor instruction trace
- Supports advanced, signal-level hardware cross-triggering between the CPU and FPGA logic domains, enabling software execution to stop on any FPGA hardware event and hardware execution to stop on any software event
- ARM Streamline Performance Analyzer with performance counters from the SoC and FPGA domains to enable full system-level analysis
- Requires only a single cable for the DS-5 Debugger and other Altera JTAG-based tools to the Altera SoC target via the Altera USB-Blaster II cable or the ARM DSTREAM™ debug and trace unit.

SoC Yocto Project-Powered Embedded Linux

Altera and its open source partners provide easily downloadable software for Altera SoC devices to enable Linux-based application development. Based on the Yocto Project, Linux for Altera SoC devices gives you a smooth transition to commercial Linux distributions.

Our SoC is one of the first ARM platforms supported in the multiplatform Linux 3.7 kernel. This enables the new kernel to not only target multiple platforms, but also to be more in line with its x86 counterpart.

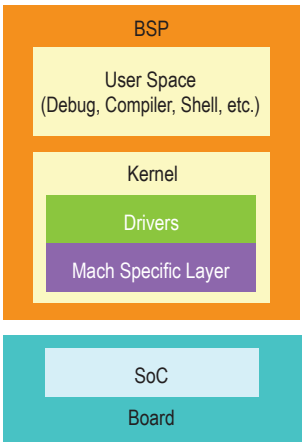
Features and Benefits:

- Prebuilt Binaries - Save time and start programming more quickly
- Latest Stable Kernel – Keep up to date with the latest bug fixes, features, and security patches
- Kernel and U-Boot code for SoC upstreamed – Community maintained code
- Multiplatform Kernel – Build one kernel with support for multiple ARM platforms including the Altera SoC
- Yocto Project – Remove cost and complexity on building your application, leaving you more time to spend on product differentiation

SoC Linux Board Support Package (BSP)

The Linux BSP is fully tested and integrated with a tool chain.
The board support package consists of:

- U-Boot with Device Tree support
- Kernel with Device Tree support
- Drivers for SoC and board components
- SoC machine specific layer
- Root File System for software developers
- GNU cross compiler for ARM architecture
- Yocto Project-based build environment



SoC Linux BSP Development

In addition to upstreaming, we update our code base against new versions of kernel.org. We also pull bug fixes and security patches from the stable branch of kernel.org. Since upstreaming takes time, customers can have our updates and upgrades faster from our staging tree, our public git tree.

Mainline

We provide a stable release from the community where customers can go to kernel.org and download the latest stable release. The scope of mainline applies to all three primary components of our Linux solution

- U-boot - denx.de
- Linux kernel - kernel.org
- File system - Yocto Project

Each component has its own “mainline” consisting of well documented development flows, release schedules, git trees and maintainers.

Common Development Tools Make Design Easier

Software Tools

A set of common software tools and design resources equips you to swiftly turn your concepts into revenue-generating applications. Our SoCs inherit the rich software development ecosystem available for ARM Cortex-A9 MPCore processors, including software development tools, operating systems, and middleware. This ecosystem compatibility ensures you can stay productive with familiar tools and reuse legacy software to shorten the development cycle.

You can follow the same software development process for our SoC devices that you do with other embedded processors. Altera and its ecosystem partners provide tool choices for each step of the process, from board bring-up to building Linux kernels to debugging application software.

We provide comprehensive operating system (OS) support including Linux, Wind River VxWorks, and more. Using our reference Linux kernel or board support packages for other operating systems, you can immediately start OS-based application development.

For development tools, you can use the Altera SoC Embedded Design Suite for hardware-to-software handoff, Linux development, bare-metal usage, and FPGA-adaptive debugging.

Hardware Tools

Our productivity-enhancing Quartus II software development environment, featuring the Qsys system integration tool, makes development easier for hardware designers. Qsys saves you time and effort in the FPGA design process, simplifying development of complex hardware systems.

Faster Development

- Easy-to-use GUI interface enables quick integration of IP functions and subsystems
- Automatic generation of interconnect logic and automatic HDL generation of your system
- Hierarchical design flow enables scalable designs, supports team-based design, and maximizes design reuse
- Support for a wide range of IP interface standards including ARM AMBA®/AXI, Avalon® Memory-Mapped, and Avalon Streaming interfaces
- Automatic generation of a simulation model, software header file, and data sheet to expedite development across hardware and software teams

Faster Timing Closure

- High-performance Qsys interconnect based on the network-on-a chip (NoC) architecture
- User control of pipelining to meet f_{MAX} and latency system requirements

Faster Verification

- Automatic testbench generation and verification IP suite let you start your simulation faster
- Ability to bring your board up faster by sending read and write transactions into a live system for debug

Ready to Learn More?

With Altera's ARM-based SoCs, you can reduce board size, system power, and system cost while increasing system performance. Our 28 nm portfolio continues to reinvent programmable logic, enabling you to create differentiated and more complex solutions with less time and effort. If you're ready to learn more, contact your local Altera representative or visit our website for white papers, webcasts, and technical details on our SoCs.

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