IGLOO®2 FPGAs

Up to 150K LEs | DSP | 5G SERDES | PCI Gen2 | XAUI | I/O Density

Lowest System Cost

Best-in-Class Integration

Low Power

Reliability

Security

Microsemi

IGLOO2 FPGAs

Microsemi's IGLOO®2 FPGAs offer best-in-class feature integration coupled with the lowest power, highest reliability and most advanced security in the industry. The device's high level of integration provides the lowest total system cost versus competitive FPGAs while improving reliability, significantly reducing power and providing unparalleled security.

Microsemi Leadership in:

Best-In-Class Integration*

- Highest number of 5G transceivers
- Highest number of GPIO
- Highest number of PCI compliant 3.3V I/O
- Only FPGA with hardened memory subsystem
- Only non-volatile and instant-on mainstream FPGA

Low Power FPGAs

- 10X lower static power
- 25% lower total power
- 5X Lower SERDES Power

Reliable FPGAs

- Only FPGA with SEU immune fabric and mainstream features
- Extended temperature support (up to 125ºC Tj)

Secure FPGAs

- Built-in state-of-the-art design security for all devices
- Root of trust

All at the Lowest Total System Cost

Integration

Low Power

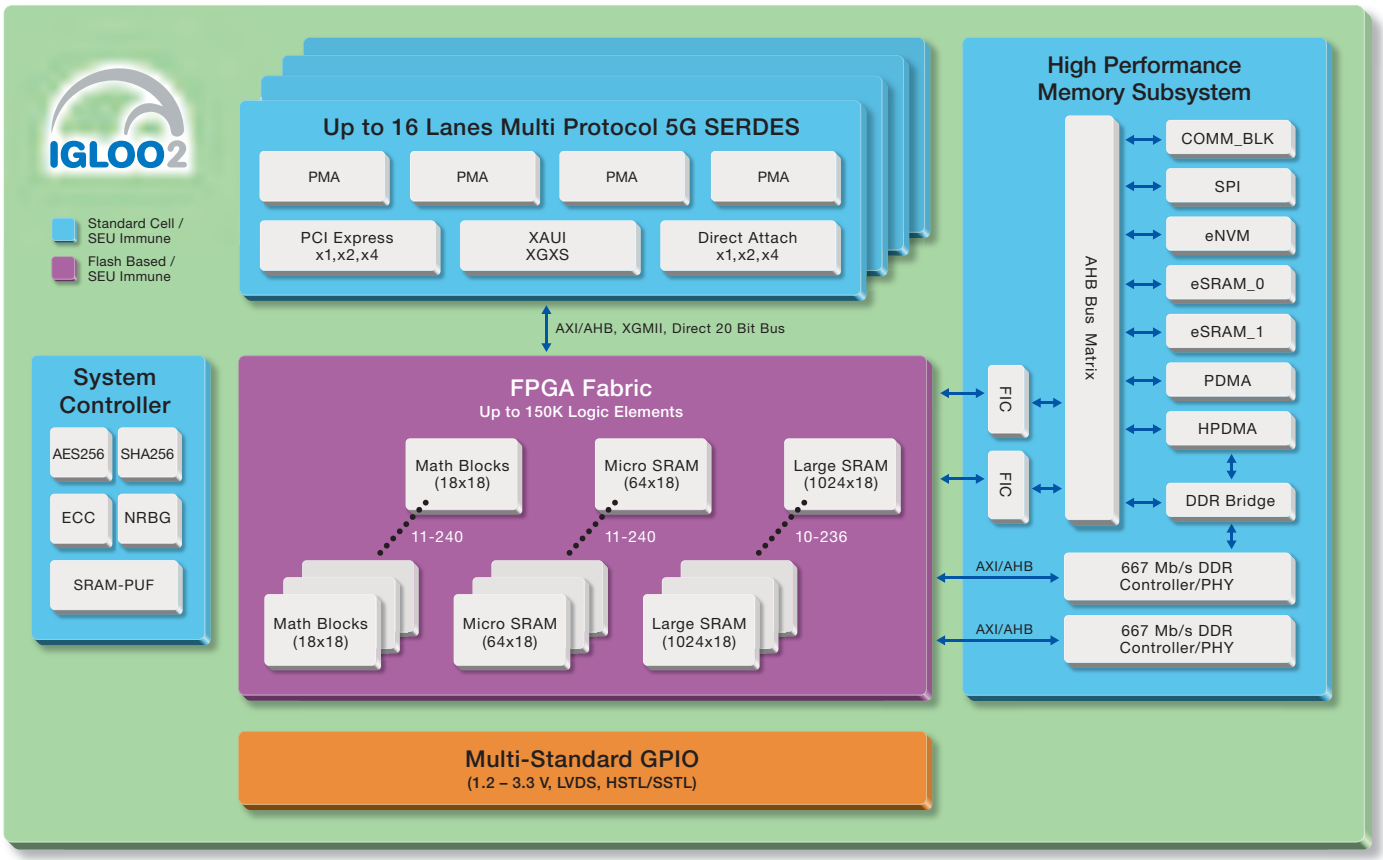
Reliability

Secure

*When compared to competitive FPGAs under 150K LEs with 5G SERDES

IGLOO2 FPGA Block Diagram

Microsemi's IGLOO2 FPGAs provide a 4-input look-up table (LUT) based fabric, 5G transceivers, high-speed general purpose I/O (GPIO), block RAM and digital signal processing (DSP) blocks in a differentiated, cost- and power-optimized architecture. This next-generation IGLOO2 FPGA architecture offers up to 5X more logic density and 3X more fabric performance than its predecessors and combines a non-volatile flash-based fabric with the highest number of GPIO, 5G serialization/deserialization (SERDES) interfaces and PCI Express® (PCIe®) endpoints when compared to other products in its class.



Acronyms

AES — Advanced Encryption Standard

AHB — Advanced High-Performance Bus

APB — Advanced Peripheral Bus

AXI — Advanced eXtensible Interface

DDR — Double Data Rate

DPA — Differential Power Analysis

ECC — Elliptical Curve Cryptography

EDAC — Error Detection and Correction

FDDR — DDR2/3 Controller in FPGA Fabric

FIC — Fabric Interface Controller

HPMS — High Performance Memory Subsystem

IAP — In-Application Programming

MACC — Multiply-Accumulate

MDDR — DDR2/3 Controller in HPMS

SECDED — Single Error Correct Double Error Detect

SEU — Single Event Upset

SHA — Secure Hashing Algorithm

XAUI — 10 Gbps Attachment Unit Interface

XGMII — 10 Gigabit Media Independent Interface

XGXS — XGMII Extended Sublayer

IGLOO2 FPGA Architecture

This next-generation IGLOO2 FPGA architecture offers up to 150K logic elements (LEs), implemented with 4-input LUT with carry chains, giving 2X performance, and includes multiple embedded memory options and math blocks for DSP. High-speed serial interfaces include PCIe, 10 Gbps attachment unit interface (XAUI) / XGMII extended sublayer (XGXS) plus native SERDES communication, while double data rate 2 (DDR2)/DDR3 memory controllers provide high speed memory interfaces.

High-Performance FPGA

- Efficient 4-input LUTs with register and carry chains for high performance and low power
- Up to 236 blocks of dual-port 18 Kbit SRAM (large SRAM) with 400 MHz synchronous performance (x18, x9, x4, x2, x1)
- Up to 240 blocks of three-port 1 Kbit SRAM with 2 read ports and 1 write port (micro SRAM)
- High performance DSP signal processing
  - Up to 240 fast math blocks with 18x18 signed multiplication, 17x17 unsigned multiplication and 44-bit accumulator

High-Speed Serial Interfaces

- Up to 16 SERDES lanes, each supporting:
  - XGXS/XAUI extension (to implement a 10 Gbps (XGMII) Ethernet PHY interface)
  - Native SERDES interface facilitates implementation of Serial RapidIO in fabric or other protocols such as JESD204B, SGMII, etc.
  - PCIe endpoint controller x1, x2, x4 lane PCIe core up to 2 Kbytes maximum payload size 64-/32-bit AXI/AHB master and slave interfaces to the application layer

High-Speed Memory Interfaces

- Up to 2 high speed DDRx memory controllers
  - HPMS DDR (MDDR) and Fabric DDR (FDDR) controllers
  - Supports LPDDR/DDR2/DDR3
  - Maximum 333 MHz clock rate
  - SECDED enable/disable feature
  - Supports various DRAM bus width modes, x8, x9, x16,x18, x32, x36
  - Supports command reordering to optimize memory efficiency
  - Supports data reordering, returning critical word first for each command

Reliability

- Single event upset (SEU) immune
  - Zero FIT FPGA configuration cells
- Junction temperature:
  - 125°C – Military temperature
  - 100°C – Industrial temperature
  - 85°C – Commercial temperature
- Single error correct double error detect (SECDED) protection on the following:
  - Embedded memory (eSRAMs)
  - PCIe buffer
  - DDR memory controllers with optional SECDED modes
- Buffers implemented with SEU resistant latches on the following:
  - DDR bridges (HPMS, MDDR, FDDR)
  - SPI FIFO
  - COMM_BLK
- NVM integrity check at power-up and on-demand
- No external configuration memory required
  - Instant-on, retains configuration when powered off

Security

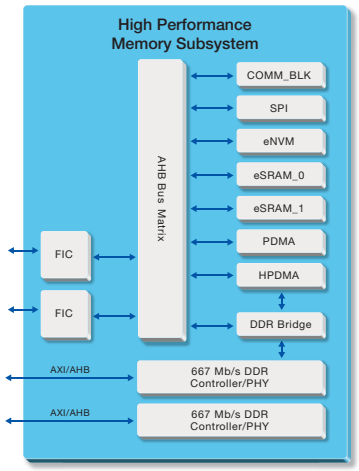
- Design security features (available on all devices)
  - Intellectual property (IP) protection via unique security features and use models new to the PLD industry
  - Encrypted user key and bitstream loading, enabling programming in less-trusted locations
  - Supply-chain assurance device certificate
  - Enhanced anti-tamper features
  - Zeroization
- Data security features (available on premium devices)
  - Non-deterministic random bit generator (NRBG)
  - User cryptographic services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) Engine)
  - User physically unclonable function (PUF) key enrollment and regeneration
  - Cryptographic Research Inc. (CRI) pass-through DPA patent portfolio license
  - Hardware firewalls protecting microcontroller subsystem (HPMS) memories

Low Power

- Low static and dynamic power
  - Flash*Freeze mode for fabric
- 10X lower static power
- 25% lower total power
- 5X lower SERDES power

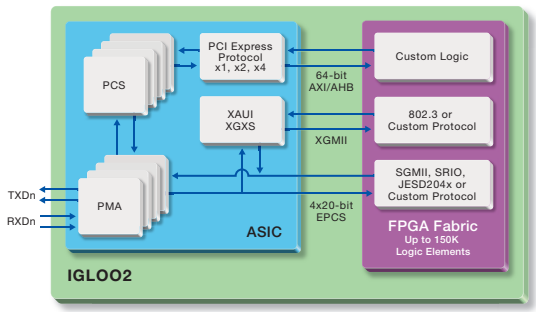
IGLOO2 FPGA Features

High-Performance Memory Subsystem



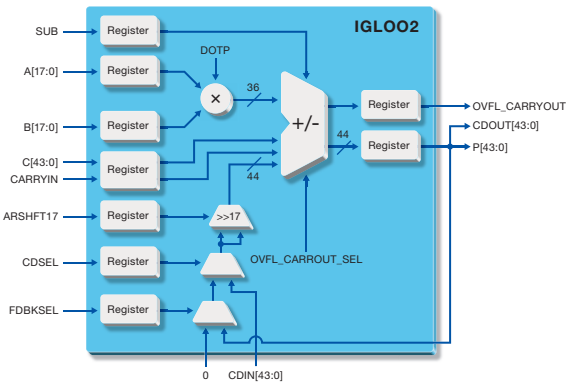
- 64 KB embedded SRAM (eSRAM)
- Up to 512 KB embedded nonvolatile memory (eNVM)
- One SPI/COMM_BLK
- DDR bridge (2 Port) with 64-Bit AXI interface
- Non-blocking, multi-layer AHB bus matrix allowing multi-master scheme supporting 4 masters and 8 slaves
- Two AHB/APB interfaces to FPGA fabric (master/slave capable)
- Two DMA controllers to offload data transactions
  - 8-channel peripheral DMA (PDMA) for data transfer between soft peripherals in fabric and embedded eSRAMs as well as support for memory to memory transfers
  - eSRAM and external DDR memory for efficient data movement between embedded real time memories

IGLOO2 FPGA SERDES



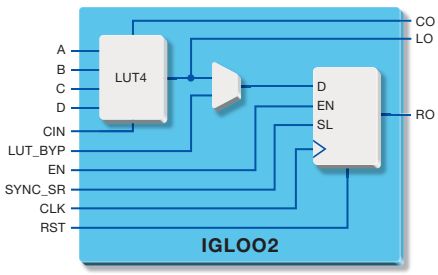
- Up to 16 lanes at up to 5Gbps
- Dual based reference clocks with single-lane rate granularity
  - Tx and Rx PLLs programmable for each lane
  - Reference clock is shared per groups of two lanes
- Transmitter features
  - Programmable pre/post-emphasis
  - Programmable impedance
  - Programmable amplitude
- Receiver features
  - Programmable termination
  - Programmable linear equalization
- Built-in system debug features
  - PRBS gen/chk
  - Constant patterns
  - Loopbacks

IGLOO2 FPGA MathBlocks



- High-performance and power optimized multiplications operations
- Supports 18x18 signed multiplication natively
- Supports 17x17 unsigned multiplications
- Supports dot product: the multiplier computes (A[8:0] x B[17:9] + A[17:9] x B[8:0]) x 29 Independent third input C with data width 44-bits completely registered
- Supports both registered and unregistered inputs and outputs
- Internal cascade signals (44-bit CDIN and CDOUT) enable cascading of the mathblocks to support larger accumulator, adder, and subtractor without extra logic
- Supports loopback capability
- Adder support: (AxB) + C or (AxB) + D or (AxB) + C + D
- Clock-gated input and output registers for power optimizations

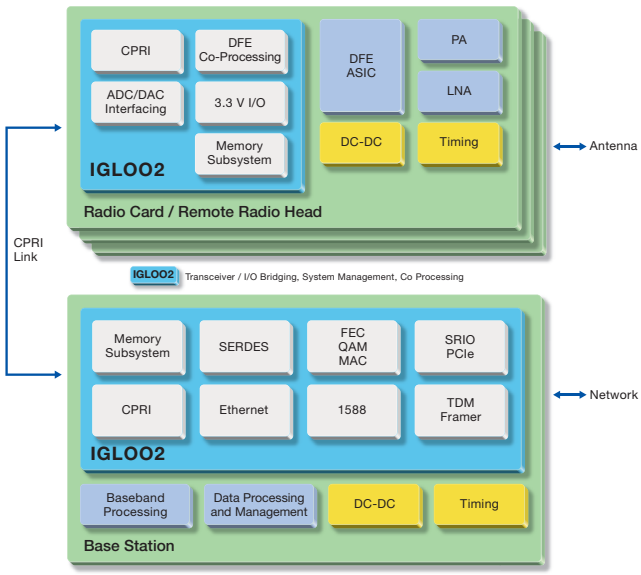
IGLOO2 FPGA LEs



- A fully permutable 4-input LUT
- A dedicated carry chain based on the carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT
- Clock-gated input and output registers for power optimizations

IGLOO2 FPGA Applications

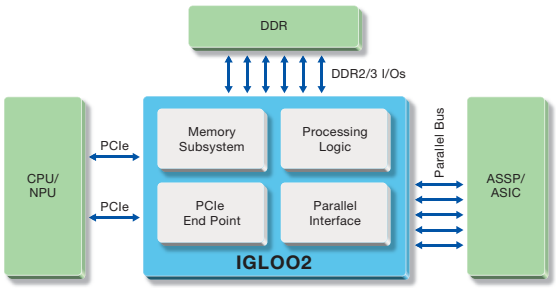
Wireless



Architects of carrier wireless systems—specially outdoor systems like remote radio heads and microwave systems—need FPGA devices that can not only consume lower power but also sustain performance with extended temperatures. Microsemi IGLOO2 FPGA provides lower power consumption with options to support extended temperature range with sustained performance.

- SERDES to support CPRI, ADC/DAC, SRIO and GbE
- High density GPIO for I/O expansion
- 3.3V I/O for SFP and RF devices
- DSP for DFE and BB co-processing

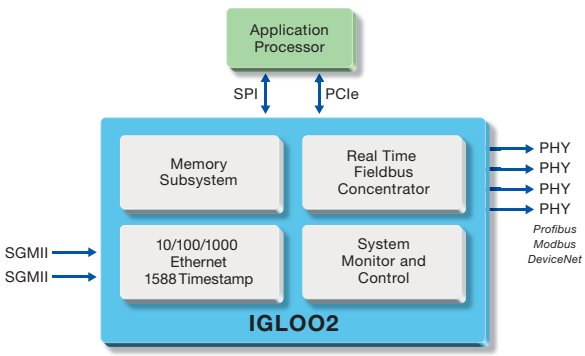
Wireline



Customers designing state-of-the-art wireline systems like Edge Routers and Optical Transport Networks (OTNs), need a large number of I/Os to control and manage power, fans, displays and other peripherals. Microsemi IGLOO2 FPGAs provide high GPIO count with 3.3V supply and PCI Express gen 1 & 2 capability.

- SERDES for PCIe, GbE, 10GbE bridging
- High density GPIO for I/O expansion
- Mainstream FPGA fabric for co-processing in IPSec, QoS and traffic management applications

Industrial Networking & Control

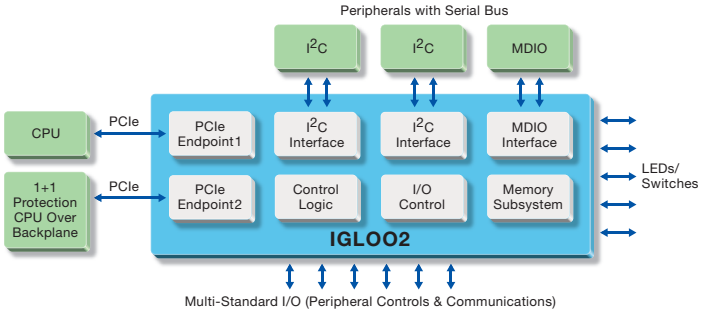


IGLOO2 FPGAs support a broad range of interfacing capabilities and a large number of I/Os, making them the ideal FPGA choice for implementing today's industrial networking and control protocols. The highly reliable FPGA fabric with built-in SERDES and flexible I/O with hysteresis are ideally suited to meet the requirements for the industrial market.

- SERDES and GPIO for multiple Ethernet based interfaces (GbE, 1588, Industrial Ethernet)
- PCIe endpoints for interfacing to application and host processor
- Best-in-Class security and reliability for safety critical, secure system monitor and control applications

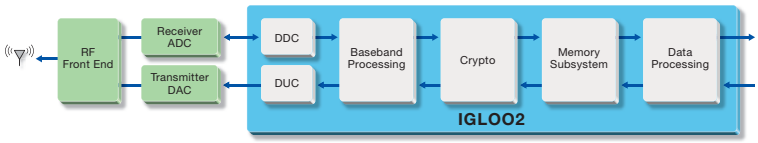
System Management

For designers of complex, high availability systems; IGLOO2 FPGAs are a reliable system management solution that provides superior uptime. From power supply sequencing to I/O expansion to fan control to reset management to booting the host CPU securely, every design has unique system management requirements. IGLOO2 FPGAs provide a flexible, reliable, and secure system management solution to address all aspects of today's complex system management requirements.



- Multiple PCI endpoints for switch/protect schemes
- Multi-standard GPIO for I/O expansion
- 3.3V I/O for LED, HMI and control connectivity
- Instant-on for power, system and chassis management
- Secure boot and M2M authentication

Secure Wireless



State-of-the-art-security coupled with DSP signal processing blocks and low power, offer designers of secure communications gear a single chip solution for both waveform and crypto processing.

- High speed GPIO for ADC/ DAC interfacing and HMI
- DSP and mainstream fabric for baseband processing
- Best–in-class security for secure data communications and anti-tamper
- Ultra-low static power for portability

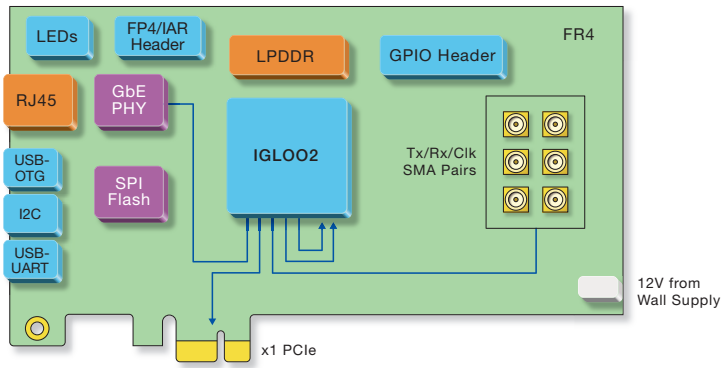
IGLOO2 FPGA Design Resources

Design Software

System designers can leverage the newly released, easy-to-use Libero® system-on-chip (SoC) software for designing IGLOO2 devices. Libero SoC integrates industry leading synthesis, debug and DSP support from Synopsys, and simulation from Mentor Graphics with power analysis, timing analysis and push button design flow.

Design Hardware

Microsemi's IGLOO2 Evaluation Kit gives designers access to IGLOO2 FPGAs which offer leadership in I/O density, security, reliability and low power into mainstream applications. The IGLOO2 Evaluation Kit supports industry-standard interfaces including Gigabit Ethernet, USB 2.0 OTG, SPI, I2C and UART. The kit can be used with Microsemi's Libero SoC v11.0 software, which includes a free Libero Gold license and comes preloaded with a demo. The kit can be powered through a 12V power supply or the PCIe connector and includes a FlashPro4 programmer.



Description	Quantity
IGLOO2 FPGA 10K LE	1
12V wall-mounted power supply	1
FlashPro4 JTAG programmer for programming and debugging of IGLOO2	1
(up to 1A) to PC	1

Note: The M2GL-EVAL-KIT is RoHS compliant.

IGLOO2 FPGA Product Family

IGLOO2 Devices

	Features	M2GL005	M2GL010	M2GL025	M2GL050	M2GL090	M2GL100	M2GL150
Logic/DSP	Maximum Logic Elements (4LUT + DFF)*	6,060	12,084	27,696	56,340	86,316	99,512	146,124
	Math Blocks (18x18)	11	22	34	72	84	160	240
	PLLs and CCCs	2		6			8	
	SPI/HPDMA/PDMA	1 each						
	Fabric Interface Controllers (FICs)	1			2			
	Security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (K Bytes)	128	256			512		
	LSRAM 18 K Blocks	10	21	31	69	109	160	236
	uSRAM 1 K Blocks	11	22	34	72	112	160	240
	eSRAM (K Bytes)	64						
	Total RAM (K bits)	703	912	1104	1826	2586	3552	5000
High Speed	DDR Controllers	1×18			2×36	1×18	2×36	
	SERDES Lanes (T)	0	4		8	4	8	16
	PCIe End Points	0	1		2			4
User I/O	MSIO (3.3 V)	115	123	157	139	306	292	292
	MSIOD (2.5 V)	28	40	40	62	40	106	106
	DDRIO (2.5 V)	66	70	70	176	76	176	176
	Total User I/Os	209	233	267	377	425	574	574

Note:
** Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 Fabric UG for details.*
** Feature availablility is package dependent*

I/Os per Package

IGLOO2	FCS325		VF256		VF400		FCV484		VQ144		FG484		FG676		FG896		FC1152	
Pitch (mm)	0.5		0.8		0.8		0.8		0.5		1.0		1.0		1.0		1.0	
Length x Width (mm)	11x11		14x14		17x17		19x19		20x20		23x23		27x27		31x31		35x35	
Device	**I/O**	**Lanes**	**I/O**	**Lanes**	**I/O**	**Lanes**	**I/O**	**Lanes**	**I/O**	**Lanes**	**I/O**	**Lanes**	**I/O**	**Lanes**	**I/O**	**Lanes**	**I/O**	**Lanes**
M2GL005 (S)	–	–	–	–	171	–	–	–	83[1]	–	209	–	–	–	–	–	–	–
M2GL010 (S/T/TS)	–	–	148[1]	2[1]	195	4	–	–	75[1]	–	233	4	–	–	–	–	–	–
M2GL025 (S/T/TS)	180	2	148[1]	2[1]	207	4	–	–	–	–	267	4	–	–	–	–	–	–
M2GL050 (S/T/TS)	200	2	–	–	207	4	–	–	–	–	267	4	–	–	377	8	–	–
M2GL090 (S/T/TS)[2]	200[1]	4[1]	–	–	–	–	–	–	–	–	267	4	425	4	–	–	–	–
M2GL100 (S/T/TS)	–	–	–	–	–	–	273[1]	4[1]	–	–	–	–	–	–	–	–	574	8
M2GL150 (S/T/TS)	–	–	–	–	–	–	273[1]	4[1]	–	–	–	–	–	–	–	–	574	16

Note:
** Preliminary*

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