MachXO2 Family

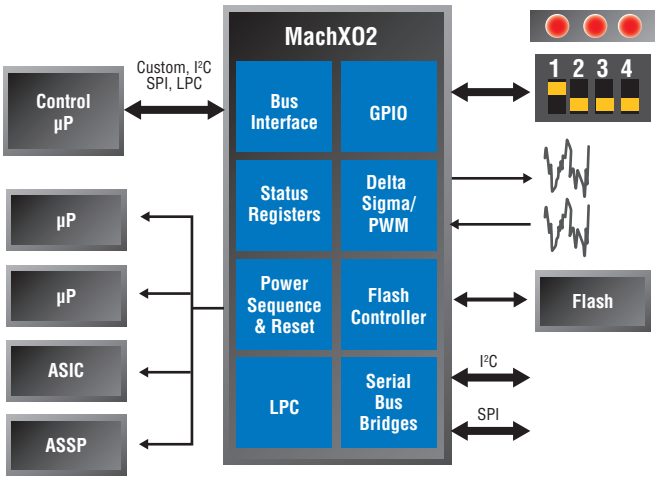
Low Cost, Low Power PLD

The MachXO2™ family of non-volatile infinitely reconfigurable Programmable Logic Devices (PLDs) is designed for applications such as telecommunications infrastructure, computing, industrial, medical equipment and consumer. Combining an optimized look-up table (LUT) architecture with 65-nm embedded Flash process technology, MachXO2 devices provide a flexible “do-it-all” solution for system designs.

The MachXO2 family offers designers the benefits of increased system integration, improved system robustness and reduced static power consumption. In addition, the MachXO2 family includes hardened implementations of some of the most popular functions used in system applications such as User Flash Memory (UFM), I²C, SPI and timer/counter.

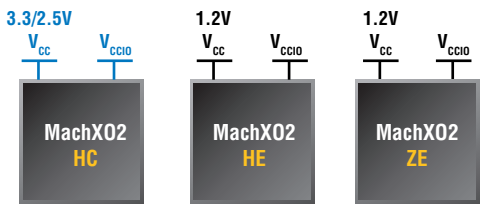
MachXO2 devices are available in three options: high performance (HC, HE) and ultra-low power (ZE).

MachXO2 Application Example



Three Product Options – More Flexibility

Focus	Option	Regulator	Nominal Vcc (V)	Internal Vcc (V)	System Performance (MHz)
High Performance	HC	✔	3.3, 2.5	1.2	150
	HE	—	1.2	1.2	150
Low Power	ZE	—	1.2	1.2	60



Key Features and Benefits

- **Large Number of Low-Cost I/Os**
  - Up to 335 I/Os with broad range of package options
- **Robust Architecture For Reliable Operation**
  - Instant-on, powers up in less than 1ms
  - Operate from a single 3.3/2.5/1.2V supply
  - Input hysteresis allows operation in noisy environment
- **High Functional Integration For Cost Reduction**
  - Densities ranging from 256 to 6864 LUTs
  - Up to 240 Kbits sysMEM™ Embedded Block RAM
  - Up to 54 Kbits Distributed RAM
  - Up to 256 Kbits of User Flash Memory
  - Hardened I²C, SPI, timer/counter functions
  - Robust PLL with fractional division
- **Flexible sysIO™ Buffer**
  - Support for LVCMOS, LVTTL, LVDS, SSTL, HSTL interfaces
  - Hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **Pre-Engineered Source Synchronous I/O**
  - Dedicated gearing logic (7:1, 4:1, 8:1)
  - Generic DDR, DDRX2, DDRX4
  - Dedicated DDR/DDR2/LPDDR with DQS support
- **System Level Support**
  - Reliable field updates with TransFR™ and Dual Boot
  - Security options include security bits, One-Time-Programmable (OTP) mode and unique device TraceID™
  - IEEE 1532 Compliant In-System Programming
  - IEEE Standard 1149.1 boundary scan
- **Broad Device Offering**
  - Commercial: 0 to 85° C (T_{JCOM})
  - Industrial: -40 to 100° C (T_{JIND})

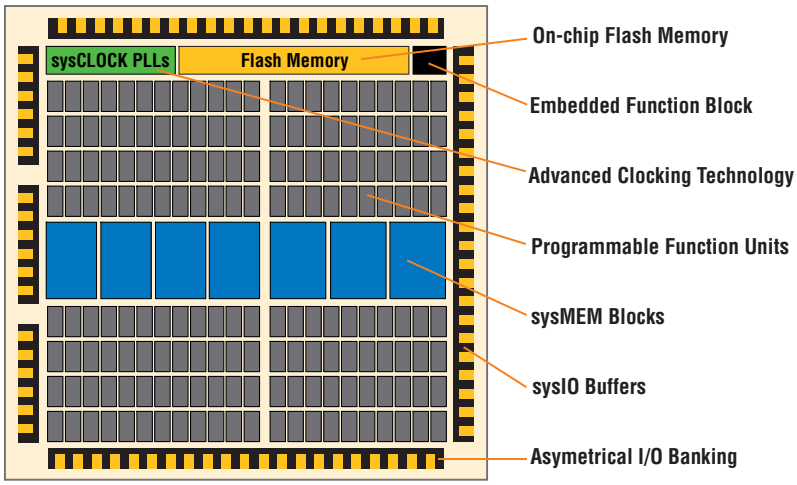
MachXO2 Architecture

Architecture Overview

MachXO2 PLDs are designed to offer an unprecedented mix of low cost and high functionality in a single device. Through the use of 65nm embedded Flash technology and innovative design, MachXO2 devices deliver high system performance, a robust architecture, support for enhanced I/O features, on-chip User Flash Memory, hardened control functions and flexible security features.

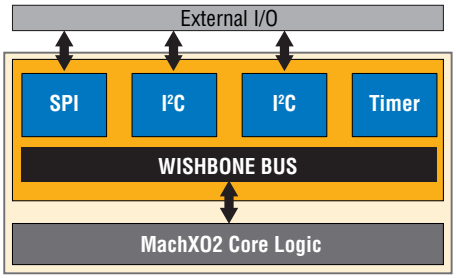
With the MachXO2 PLD family, you have everything you need to meet your low cost, high functionality and low power requirements for your next design.

MachXO2 Block Diagram



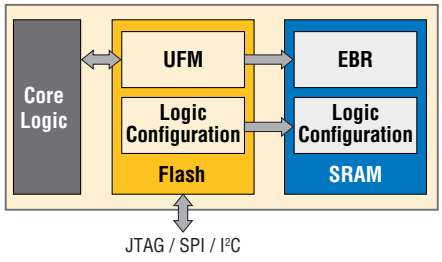
Embedded Function Block

- MachXO2 devices include hard implementations of two I²C and one SPI interface cores, and a timer/ counter
- All functions are accessible both externally and within the device



On-chip Flash Memory

- On-chip Flash memory stores both user data and device logic configuration
- Non-volatile, instant-on (less than 1ms) operation in a single device
- Up to 256Kbits of on-chip User Flash Memory (UFM)
- Non-volatile UFM storage is accessible both externally and within the device



Programmable Function Units (PFU)

- PFU blocks contain look-up tables with registered outputs that can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions
- Densities from 256 to 6864 LUTs and up to 54Kbits of distributed RAM

sysIO Buffers

- Programmable sysIO supports a wide range of interfaces
  - LVTTL, LVCMOS (3.3/2.5/1.8/1.5/1.2)
  - PCI*, LVDS*, Bus-LVDS, MLVDS
  - RSDS, LVPECL
  - SSTL 25/18, HSTL 18
- Input hysteresis
- Hot socketing
- On-chip differential termination*
- Programmable pull-up, pull-down, bus keeper (I/O cell defaults to pull-down during power-up)
- DDR registers in I/O cells
- Dedicated gearing logic

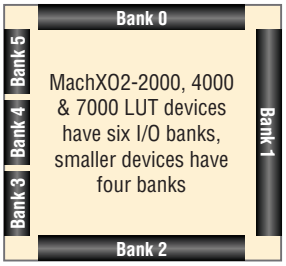
** Available on MachXO2-1200 and larger densities.*

sysMEM Embedded Block RAM Configuration Options

Single Port	True Dual Port	Pseudo-Dual Port	FIFO
8192 x 1	8192 x 1	8192 x 1	8192 x 1
4096 x 2	4096 x 2	4096 x 2	4096 x 2
2048 x 4	2048 x 4	2048 x 4	2048 x 4
1024 x 9	1024 x 9	1024 x 9	1024 x 9
		512 x 18	512 x 18

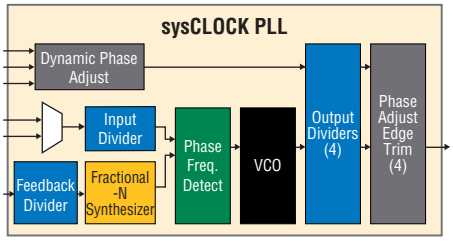
Asymmetrical I/O Banking

- Each device has asymmetrical I/O banks to flexibly connect to different interfaces



Advanced Clocking Technology

- Full featured PLL
  - Fractional division improves frequency synthesis
  - 10 - 400 MHz operation
- On-chip oscillator with +/-5% accuracy and 2-133MHz operation

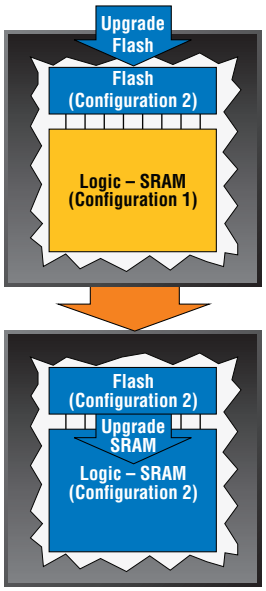


Easy, Reliable Field Updates

Lattice's Transparent Field Reconfiguration (TransFR) technology enables logic updates in the field without interrupting the operation of the system.

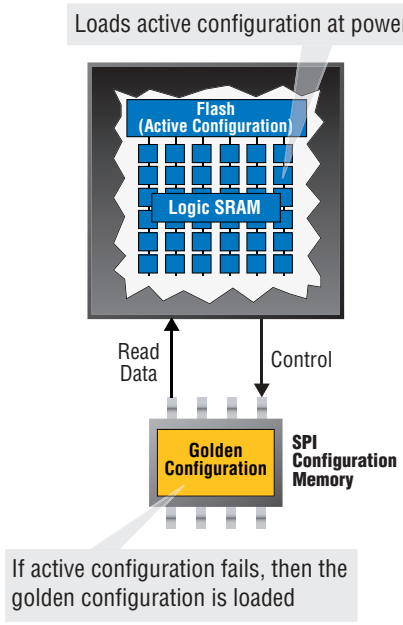
Step 1
Program Flash in background while logic functions

Step 2
Precisely control I/Os and initiate Flash to SRAM transfer through JTAG.



Dual Boot for Reliability

MachXO2 devices offer an additional level of reliability by supporting dual boot with external SPI Flash.



Programming Options

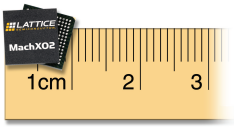
MachXO2 devices offer several programming options, including: JTAG IEEE 1149.1/1532, I²C Slave, and SPI Master/Slave modes.

Flexible Security Options

MachXO2 devices support optional security bits and a One-Time-Programmable (OTP) mode that prevents further erasure or programming of the Flash memory. A unique 64-bit device TraceID can be used for tracking purposes.

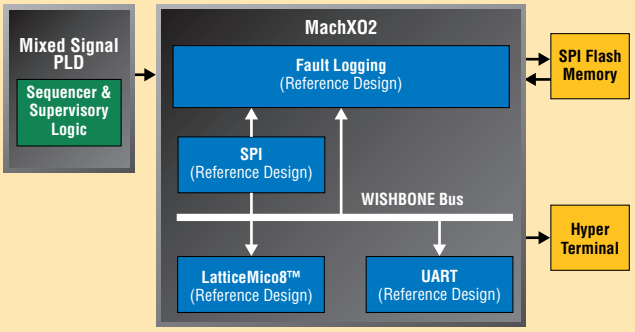
Cost and Space Saving Package Options

MachXO2 devices are available in a wide range of advanced halogen-free packages. MachXO2 devices are designed to provide density migration within the same package.

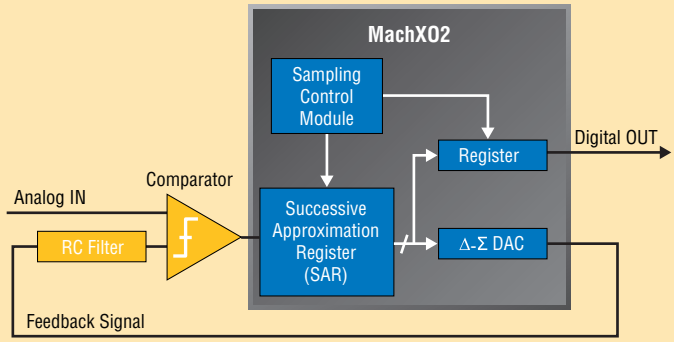


MachXO2 Application Examples

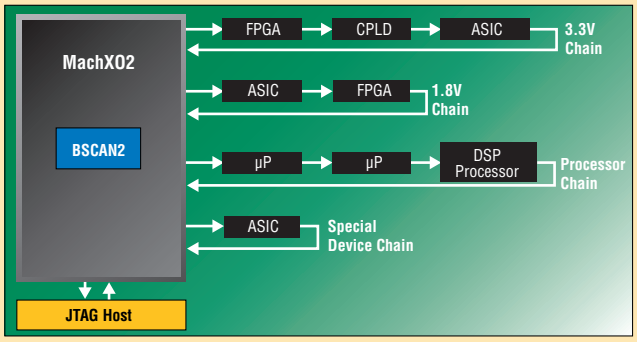
Environmental Logging



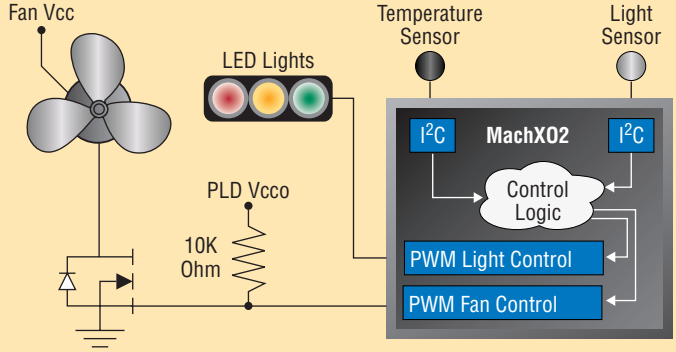
Voltage Monitoring Using Delta Sigma ADC



Boundary Scan



Fan and Light Control



Free, Easy-to-Use Lattice Software

Lattice Diamond® design tools offer a comprehensive design environment for the MachXO2 architecture and other device families. Featuring design exploration, ease of use, improved design flow, and numerous other features, Diamond allows you to complete designs faster, easier, and with better results than ever before.

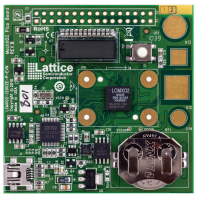
LATTICE DIAMOND DESIGN SOFTWARE

Reference Design Portfolio

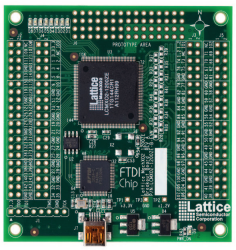
Lattice offers an expanding portfolio of IP cores and reference designs targeted for system applications. Optimized for the MachXO2 architecture, these include I²C, SPI, UART, PWM fan control, LCD controller, and the LatticeMico8™ microcontroller. The reference designs, source codes and documentation can be downloaded for free from the Lattice website. For more information, go to www.latticesemi.com/ip.

Development Kits and Evaluation Boards

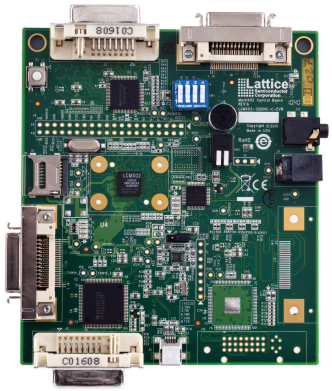
Lattice offers a number of development kits and evaluation boards that provide a complete and easy-to-use platform to evaluate the performance of the MachXO2, or aid in the development of custom designs. For more information, go to www.latticesemi.com/products/developmenthardware.



MachXO2 Pico Evaluation Board



MachXO2-1200ZE Breakout Board



MachXO2 Control Evaluation Board

MachXO2 Device Table

Feature	XO2-256	XO2-640	XO2-640U[1]	XO2-1200	XO2-1200U[1]	XO2-2000	XO2-2000U[1]	XO2-4000	XO2-7000
LUTs	256	640	640	1280	1280	2112	2112	4320	6864
EBR RAM (Kbits)	0	18	64	64	74	74	92	92	240
EBR RAM Blocks (9 Kbits/Block)	0	2	7	7	8	8	10	10	26
Distributed SRAM (Kbits)	2	5	5	10	10	16	16	34	54
User Flash Memory (Kbits)	0	24	64	64	80	80	96	96	256
PLLs	0	0	1	1	1	1	2	2	2
Package & I/O Combinations									
25-ball WLCSP (2.5 x 2.5 mm)[2]				19					
32-pin QFN (5 x 5 mm)[3]	22								
64-ball ucBGA (4 x 4 mm)	45								
100-pin TQFP (14 x 14 mm)	56	79		80		80			
132-ball csBGA (8 x 8 mm)	56	80		105		105		105	
144-pin TQFP (20 x 20 mm)			108	108		112		115	115
256-ball caBGA (14 x 14 mm)						207		207	207
256-ball ftBGA (17 x 17 mm)					207	207		207	207
332-ball caBGA (17 x 17 mm)								275	279
484-ball fpBGA (23 x 23 mm)							279	279	335
Typical Static Power									
ZE (mW)	0.019	0.033		0.070		0.098		0.153	0.230
HC (mW)	4	7	13	13	18	18	32	32	48
HE (mW)						2	3	3	5

1. Ultra high I/O count devices are supported for HC/HE options.
2. WLCSP packages are offered for ZE devices only.
3. Contact your Lattice sales representative for the support of the 32-pin QFN package.

Applications Support
1-800-LATTICE (528-8423)
503-268-8001
techsupport@latticesemi.com

Copyright © 2012 Lattice Semiconductor Corporation. Lattice Semiconductor, L (stylized) Lattice Semiconductor Corp., and Lattice (design), ispLEVER, ispVM, Lattice Diamond, LatticeMico8, MachXO2, MachXO, sysCLOCK, sysIO, sysMEM, TraceID, and TransFR are either registered trademarks or trademarks of Lattice Semiconductor Corporation in the United States and/or other countries. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

April 2012
Order #: I0221A