L A T T I C E S E M I C O N D U C T O R

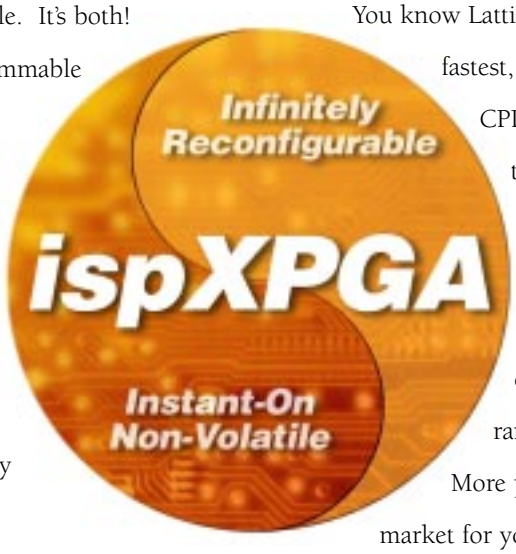
The Next Generation of FPGAs

ispXPGA™

Lattice® Semiconductor Corporation

Non-volatile and infinitely reconfigurable. It's both! Welcome to the eXpanded Field Programmable Gate Array — the Instant-On ispXPGA! ispXPGA devices offer a unique set of advantages:

- Non-Volatile/Reprogrammable in E^2
- Infinitely Reconfigurable in SRAM
- Self-Configures in Microseconds at Power-Up for "Instant-On" Availability
- Secure — No External Bitstream



You know Lattice as a supplier of the world's biggest, fastest, widest, and lowest-power ispMACH™ CPLDs, the revolutionary ispXPLD™ family, the unique ispGDX® crosspoint switch and ispPAC® programmable analog families, and ispGAL® SPLDs. Now we're adding a line of unique FPGAs in order to support you with the widest range of programmable ICs on the market. More programmability means quicker time-to-market for you.

ispXPGA Family

Family Member	System Gates	PFUs	LUT-4	Logic FFs	Block RAM	Distributed RAM	sysHSI™* Channels	User I/O	Vcc	Packaging	Body Size
ispXPGA 125/E	139K	484	1936	3.8K	92K	30K	4	160 176	1.8, 2.5, 3.3V	256 fpBGA 516 fpBGA**	17x17mm 31x31mm
ispXPGA 200/E	210K	676	2704	5.4K	111K	43K	8	160 208	1.8, 2.5, 3.3V	256 fpBGA 516 fpBGA**	17x17mm 31x31mm
ispXPGA 500/E	476K	1764	7056	14.1K	184K	112K	12	336 336	1.8, 2.5, 3.3V	516 fpBGA** 900 fpBGA	31x31mm 31x31mm
ispXPGA 1200/E	1.25M	3844	15376	30.8K	414K	246K	20	496 496	1.8, 2.5, 3.3V	680 fpSBGA** 900 fpBGA	40x40mm 31x31mm

* "E" series does not support sysHSI.
** Thermally enhanced

ispXPGA Programming and Configuration

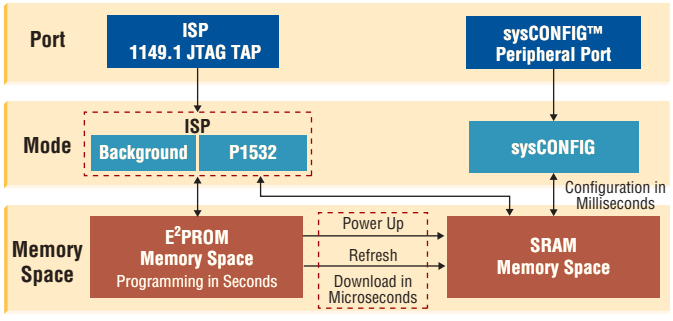
The ispXPGA family of devices takes a unique approach to FPGA configuration memory. ispXPGA devices contain two types of memory, Static RAM and non-volatile E^2CMOS® cells. The static RAM is used to control the functionality of the device during normal operation and the E^2CMOS memory cells are used to load the SRAM. The SRAM is configured either from the E^2CMOS memory or from an external source. We call this concept ispXP™, for eXpanded Programmability.

The ispXPGA family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications and the "E" series, a high performance, low cost device with no sysHSI functionality.

E^2 Nonvolatility + SRAM Reconfigurability =

- Logic available to system power-up sequence in 200 µs
- High security - no external bitstream for configuration

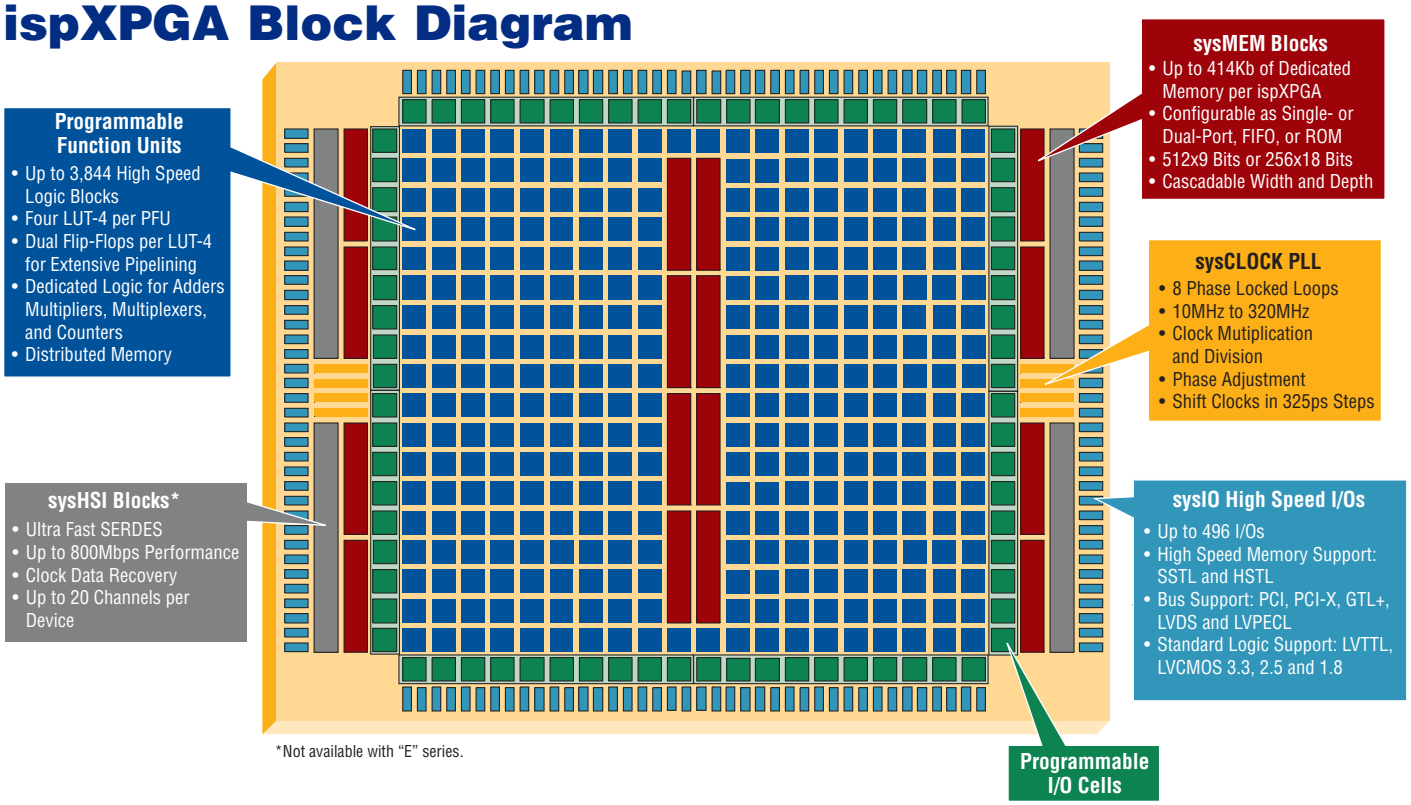
ispXPGA Configuration Modes



- Single-chip solution for reduced inventory, handling, and manufacturing costs
- No external SPROM noise, reliability, or board-space concerns

ispXPGA Architecture

ispXPGA Block Diagram

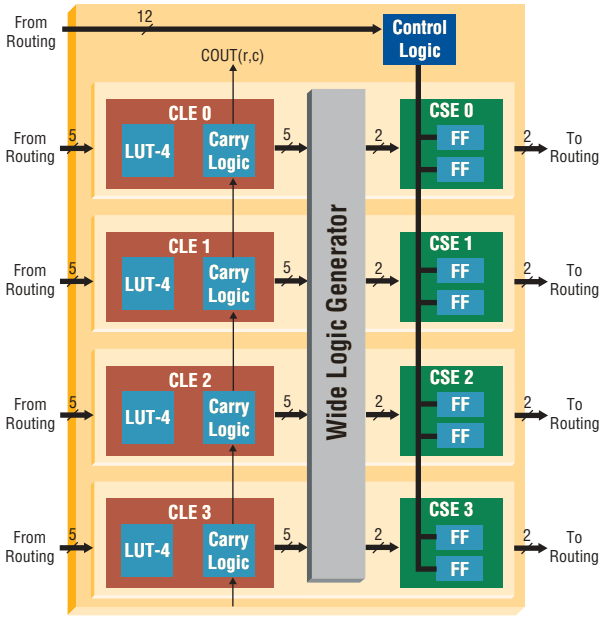


*Not available with "E" series.

Programmable Function Unit

The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions.

Programmable Function Unit Block Diagram



PFU Features

- Input Switch Matrix signals from global, general, direct-connect, and feedback routing paths
  – Up to 24 go to PFU
- Multiplexer Mode uses PFU as four 2:1 muxes, two 4:1 muxes, or one 8:1 mux, cascadable for 16:1 mux
- LUT/Carry can also be 8-bit shift register, up to 32-bits in a PFU, cascadable
- PFU's four LUT-4s configurable as two LUT-5s or one LUT-6, cascadable to LUT-7s
  – Partial functions up to 20 inputs achievable
- Wide-gating via carry chain offers 16-input OR, AND, NOR, and NAND functions, or 2-bit comparators.
- Arithmetic Mode for 4-bit adder/subtractor, magnitude comparator, or up/down pre-loadable counter
- 2 Flip-Flops per LUT for efficient pipelining and register retiming by synthesis tools
- Output Switch Matrix optimally connects PFU outputs to ispXPGA routing resources
- Memory Mode configurations
  – Single-port 64 bits
  – Dual-port 32 bits
- Set and Reset signals common to PFU's 8 FFs
- Clocks from up to 12 sources with polarity control

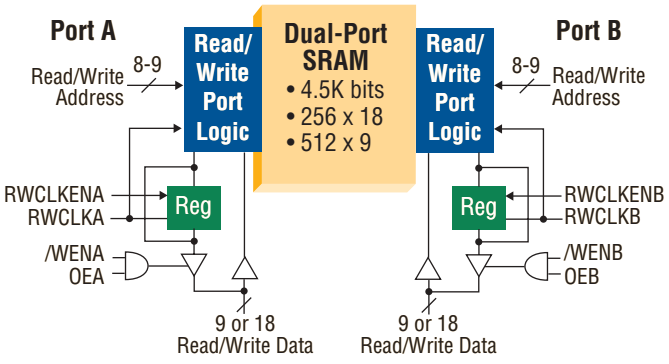
Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs. Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM™ blocks.

sysMEM Embedded Block RAM (EBR)

- Configure using ispLEVER™ software's Memory Compiler
- 4K-bit blocks usable as Single-Port, Dual-Port, FIFO, or ROM
- Byte or Word organization plus parity bit per byte
- Cascade for more depth or width
- Access times under 3 ns
- sysMEM Modes of Operation
  - Single-Port Synchronous Read/Write
  - Single-Port Synchronous Write/Asynchronous Read
  - Single-Port Synchronous Write/Synchronous Read
  - Dual-Port Synchronous Read/Write
  - Dual-Port Synchronous Write/Asynchronous Read
  - Dual-Port Synchronous Write/Synchronous Read

sysMEM Dual Port SRAM



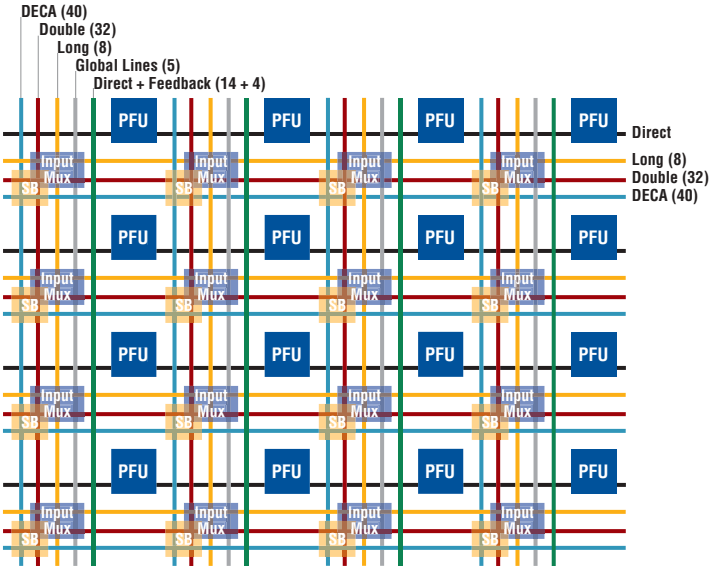
Distributed Memory

Configuration	8x1	16x1	16x2	32x1	32x2	64x1
Single-port	–	4	2	2	1	1
Dual-port	–	2	1	1	–	–
Shift Register	4	2	–	1	–	–

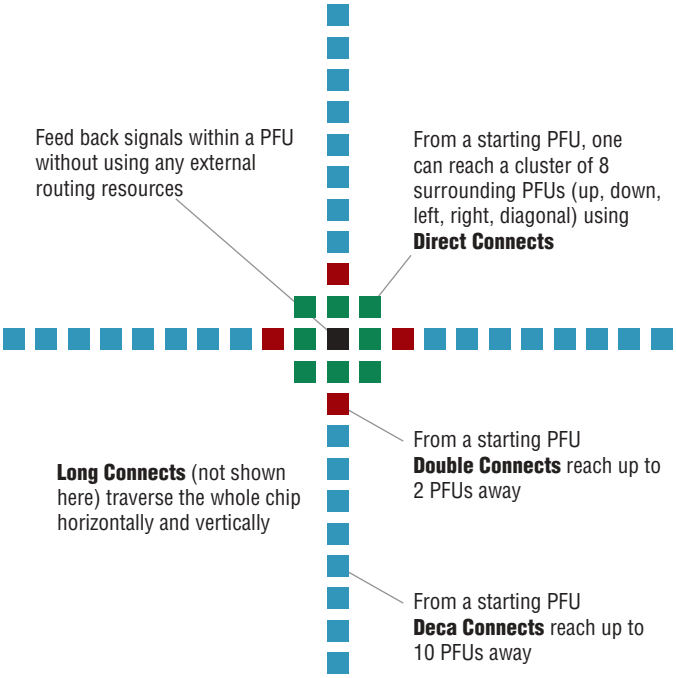
- Distributed Memory Mode of PFU's LUT
- PFU inputs become Address, Data, Write Enable and Clock
- Single-Port Synchronous Write/Synchronous Read
- Up to 64 SRAM bits per PFU
  - Single-port or Dual-port RAM
  - 8-bit shift register per LUT; 32-bit per PFU

Routing Resources

The ispXPGA architecture contains a highly flexible routing technology to connect the PFUs, PICs, and EBRs in the device. The ispXPGA's superior routing resources are optimized for fittability and performance and allow signals to be routed to any element in the device with the optimal delay.



PFU Interconnect Options



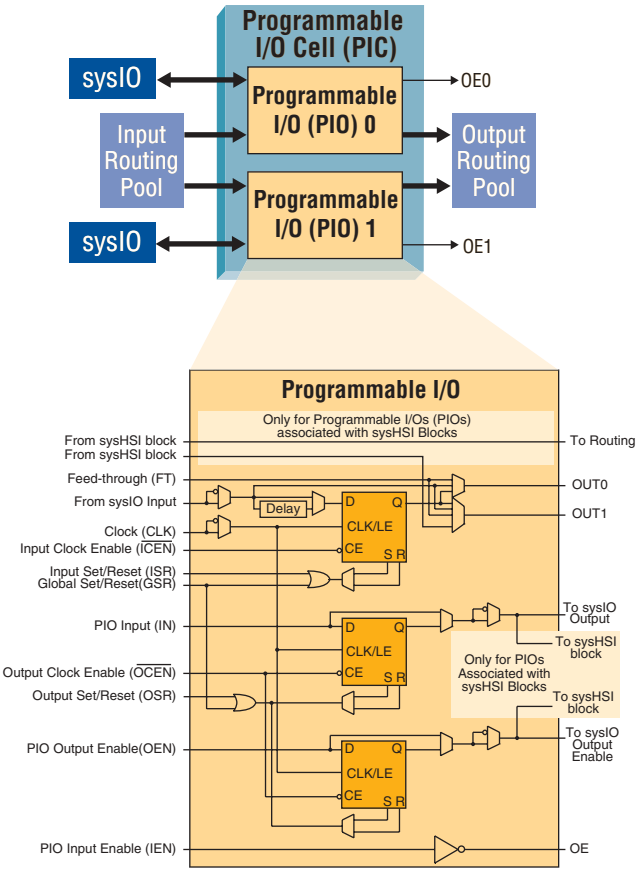
Programmable I/O Cells

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device. Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks.

Programmable I/O Features

- Separate Input, Output and OE Registers
- Flexible Set, Reset, Clock Enable and Polarity
- Input Register Offers Delay Option for Zero t_{HOLD}
- Programmable Output Slew Rate

Programmable I/O Block Diagram



sysIO™ High Speed I/O

ispXPGA devices offer up to eight sysIO banks. Each sysIO bank is capable of supporting multiple I/O standards and has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O is individually configurable based on the bank's V_{CCO} and V_{REF} settings. In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down, or a bus-keeper latch

Chip to Memory	Chip to Chip	Chip to Backplane
SSTL2 I and II	LVTTL	PCI33_3
SSTL3 I and II	LVCMOS 3.3	PCI66_3
HSTL I	LVCMOS 2.5	PCI-X
HSTL III	LVCMOS 1.8	GTL+
HSTL IV	Prog. Impedance	AGP
CTT		Bus-LVDS
↓		LVDS
SDRAM		LVPECL
DDR SRAM		
QDR SRAM		
ZBT SRAM		

sysIO Features

- Up to 8 independent sysIO banks
  - Each supports multiple I/O standards
  - Each has own I/O supply voltage (V_{CCO})
  - Each has own reference voltage (V_{REF})
  - Each bank configurable based on V_{CCO} and V_{REF}
- Configurable drive strength on each I/O
- Pull-up, pull-down, or Bus-Keeper latch capabilities for bus maintenance on each I/O

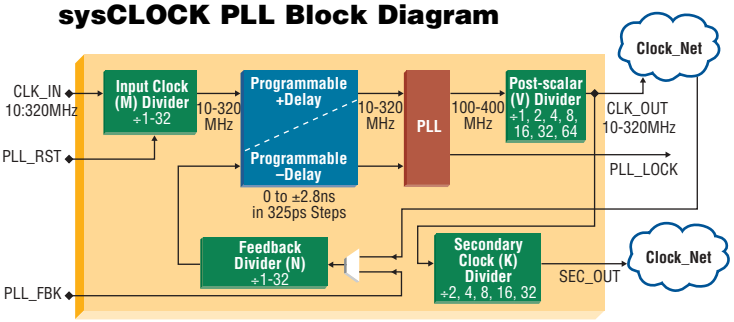
ispXPGA devices include three classes of I/O interface standards

- Un-terminated, single-ended
  - 3.3V LVTTL and 1.8V, 2.5V, and 3.3V LVCMOS
  - PCI, PCI-X, and AGP-1X
- Terminated, single-ended
  - SSTL and HSTL
  - CTT and GTL+
- Differential
  - LVDS and LVPECL

sysCLOCK™

ispXPGA devices provide up to eight sysCLOCK Phase-Locked Loops (PLLs). Lattice's advanced sysCLOCK PLL circuitry consists of PLLs plus the various dividers, reset, and feedback signals associated with PLLs. The sysCLOCK feature provides the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, sysCLOCK circuitry can generate clock signals that are aligned either at the board-level or the device-level.

sysCLOCK PLL Block Diagram



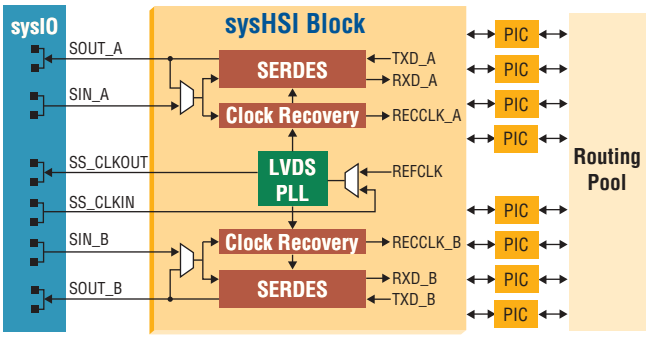
sysCLOCK PLL Features

- Eight PLLs per Device
  - Plus 8 Global Clocks
  - Plus 8 Low-Skew Clock Nets
- Clock Frequency Synthesis
- Multiple Clock Signal Generation
- Device or Board Clock Alignment
- 10 - 320MHz, t_{LOCK} 25 µs
- Jitter: Cycle-to-Cycle ±100ps; Period ±150ps; Input Jitter Tolerance ±300ps
- Four Dividers per PLL
  – M Divider for Clock Division
  – N Divider for Clock Multiplication
  – V Divider for VCO Operation at Higher Frequencies
  – K Divider for Secondary Clock Division
- Programmable Delay for Advancing or Delaying Clock
  – 325ps Increments from 0 to ±2.8ns
  – Inserts Delay on PLL Input or Feedback Lines
- PLL Input Clock from Associated Global Clock Pin
- Output Routed to Associated Global Clock Net
- Secondary Clock Divided from Primary Clock Output
- PLL Reset, Feedback, and Lock Control Signals

sysHSI High-Speed Serial Interface

Lattice's High Speed Serial Interface (sysHSI) allows high-speed serial data transfer over a pair of LVDS I/O at up to 800Mbs. The ispXPGA devices have multiple sysHSI blocks. Each sysHSI block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in each sysHSI block share a common clock and must operate at the same nominal frequency.

sysHSI Block Diagram



sysHSI Features

- sysHSI Block Performs
  – Clock data recovery (CDR)
  – Serialization
  – De-serialization
- Two Options Available
  – High performance sysHSI (standard part number)
  – Low-cost, no sysHSI ("E" series)
- Low Voltage Differential Signals (LVDS)
- Clock Signal Encoded into Serial Data Stream
- CDR used to Cancel Channel-to-Channel Skew and Data-to-Clock Skew
- Dedicated PLL per sysHSI Circuit

sysHSI High-Speed Operation Modes

Mode	Data Code	Serial Data Rate (Mbps)	Pay Load Data Rate (Mbps)	Parallel Data/Clk (MHz)	Parallel Data Width	Serial/ Parallel Ratio	Symbol Alignment Pattern	CDR Support
SERDES without Encoding/Decoding	8B/10B	400 to 800	320 to 680	40 to 85	10b Encoded	10	K28.5 +/-	CDR
SERDES with Encoding/Decoding	10B/12B	400 to 800	333 to 708	33.3 to 70.8	10b Raw Data	12	SyncPat	CDR
Source-Synchronous (n channels)	N/A	400 to 800	n x (400 to 800)	100 133 200	n x 8b n x 6b n x 4b	8 6 4	Synch to LS Clock	De-skew (optional)

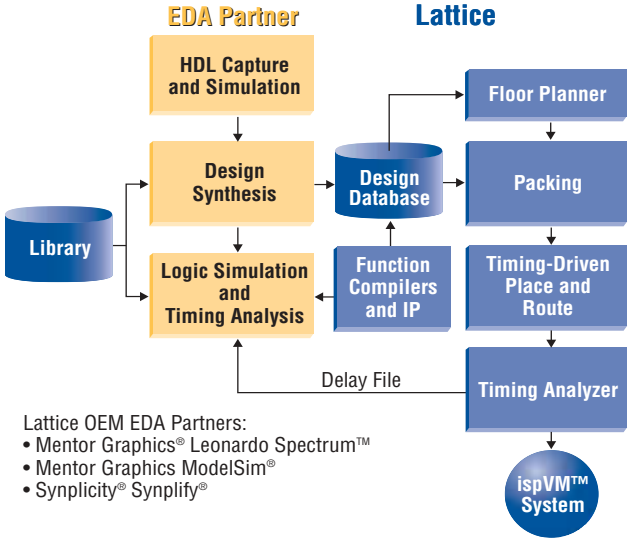
ispLEVER Design Software

Lattice's ispLEVER is a new generation of PLD design tool equipped to provide a complete system for FPSC, FPGA, ispXPLD, CPLD, ispGDX and SPLD design. ispLEVER includes a fully integrated, push-button design environment and advanced features for interactive design optimization and debug.

Features

- Fully Integrated Synthesis and RTL and Timing Simulation Tools
- Complete Design Flow for All In-System Programmable (ISP™) Lattice Device Families
- Advanced Timing-Driven Placement and Routing
- IP Manager and Module Generator
- Fast, Efficient Run Times and Competitive Device Performance and Utilization
- Supported by Libraries from Leading CAE Vendors
  - Aldec, Cadence, Innoveda, Mentor Graphics, Synopsys, Synplicity
- Windows® and UNIX® Solutions

ispLEVER Design Software Flow Chart



Lattice OEM EDA Partners:
- Mentor Graphics® Leonardo Spectrum™
- Mentor Graphics ModelSim®
- Synplicity® Synplify®

ispXPGA Select Performance

T_A = 25° C; V_{CC} = 1.8V

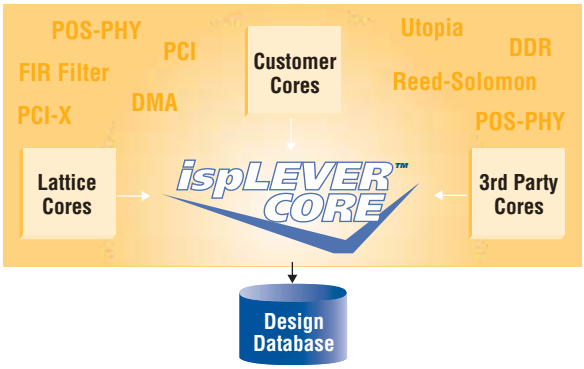
Function		Speed
4-Input LUT Delay		440ps
Synchronous Counter	8-bit	334MHz
Loadable Up/Dn Carry-Ripple Counter	64-bit	156MHz
Carry-Ripple Adder	64-bit	232MHz
Multiplexer	64:1	237MHz
De-Multiplexer	1:64	371MHz
Shift Reg Up/Dn, Circular Shift	64-bit	315MHz
Barrel Shifter	64-bit	184MHz
PLL Frequency	Min Max	10 MHz 320 MHz
LVDS with Clock Recovery	Max	850Mbit

IP Cores

Lattice's ispLEVER Core program offers a wide variety of IP cores from Lattice and third-party partners.

- Custom Macro Generation -- Reuse Your Own Earlier Work
- High Quality Lattice-developed IP Cores
  - Busses, Communications, Memory, DSP functions
  - Richly parameterized
  - Free trial versions on Lattice website
- Broad Offering from Lattice IP Partners

Lattice's ispLEVER Core Program Saves Time



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July 2004
Order #: I0141A