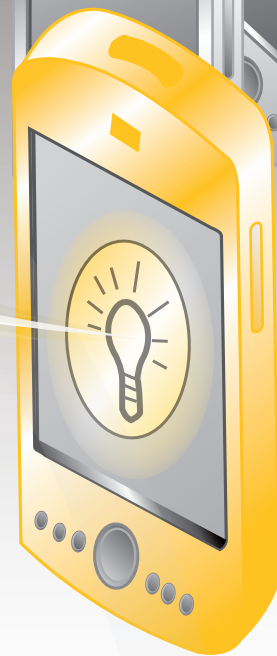# Consumer Solutions

Your Idea In Our Silicon

Lattice Semiconductor's low cost and low power FPGAs allow new handsets with new and proprietary ideas and features to be developed without waiting for next-generation chipsets.
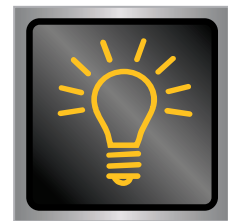
Your Added Functionality

+

LATTICE

Ultra-Low Density FPGA Platform

=

Customized Lattice Ultra-Low Density FPGA

Enable Innovative Solutions

Ultra-Low Density FPGAs Enable Differentiation

Ultra-low density FPGAs from Lattice serve as companion chips to standard Application Processors (APs), enabling consumer mobile designers to quickly and easily bring new features and capabilities to market.

- **Quickly meet new customer demand**
- **Stay ahead of the competition**
- **Create proprietary solutions**
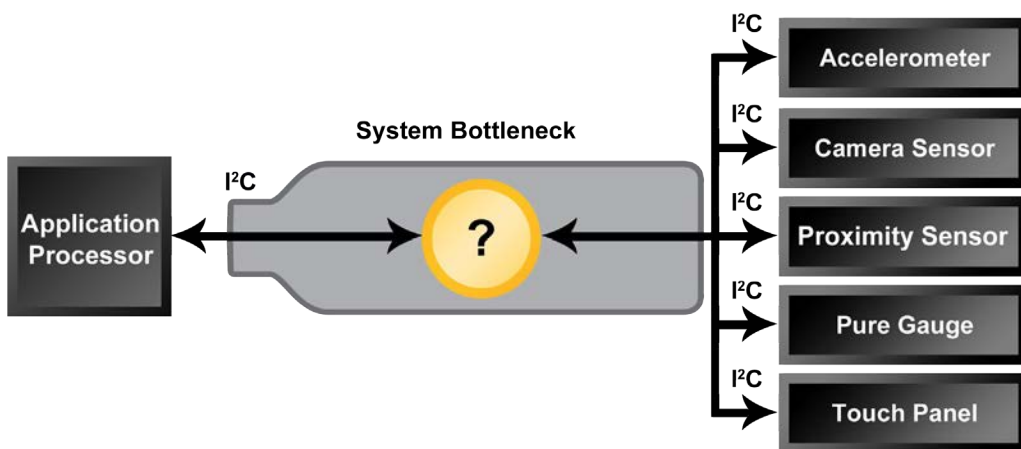- **Innovate now!**

For New Opportunities

Table of Contents

Eliminating "Sensor Choke" in Smartphones
(EBI2 to I²C Bridging)

Too many I²C devices

Smartphones now have as many as 15 to 20 sensors.

All are trying to talk to the processor through a slow I²C port.

This chokes the application processor and kills system performance.

Bridge slow I²C devices to a high-speed bus
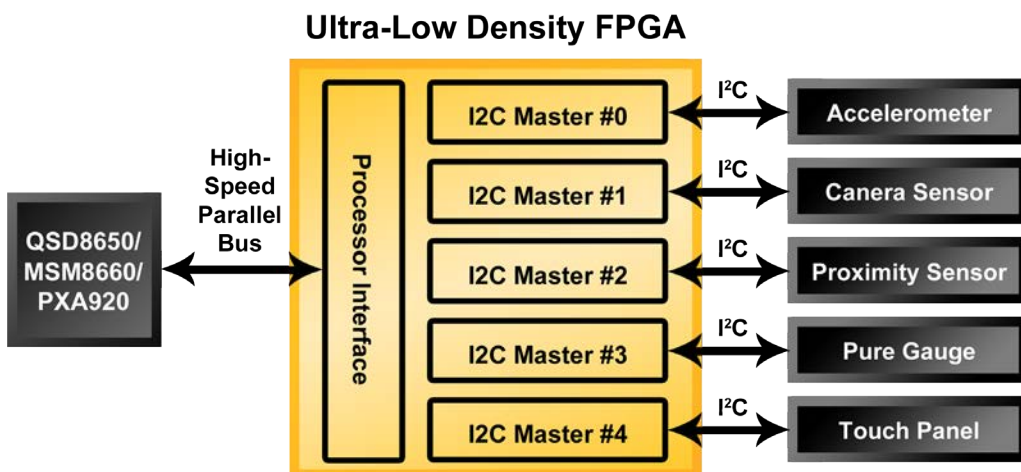
Lattice ultra-low density FPGAs can implement multiple buffered I²C controllers.

Connect them to the application processor through a high-speed parallel bus, (such as EBI2) and high-speed serial bus (such as SPI).

Smart Sensor Management for Smartphones

(Interrupt Aggregation)

Multiple sensor interrupts slow down smartphone responses
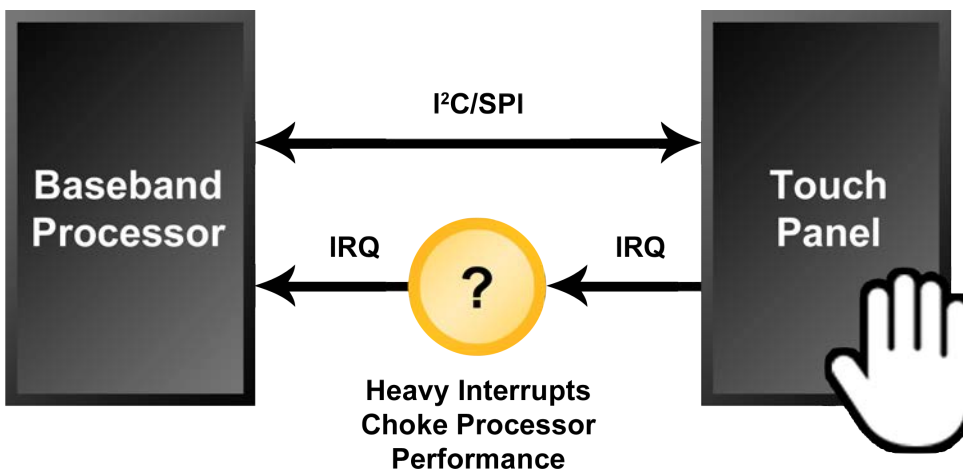
Multi-touch screens can generate very heavy interrupts at a given time.

This tremendously increases processor overhead and potentially affects other tasks.

Interrupt aggregator offloads processor and improves performance
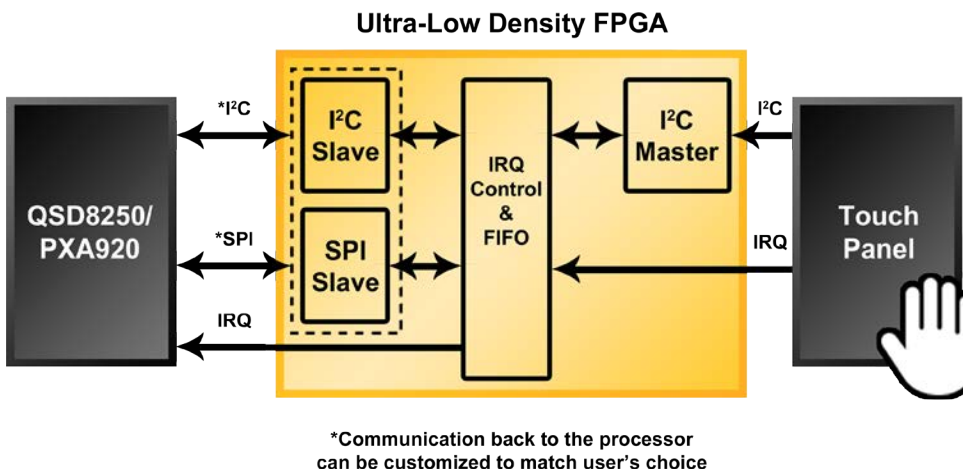
Lattice ultra-low density FPGAs can aggregate multiple sensor interrupts into efficient summaries to offload the processor.

The interface to the processor (red dotted box) can be customized to any available interface such as SPI or a processor local bus' offering extra flexibility in terms of design integration.

*Communication back to the processor can be customized to match user's choice

Smart Sensor Management for Smartphones
(Auto-Polling)

Sensor polling increases processor overhead

Baseband Processor ←I²C→ **?** ←I²C→ **Gyroscope**

Processor Needs to Constantly Poll the Sensor
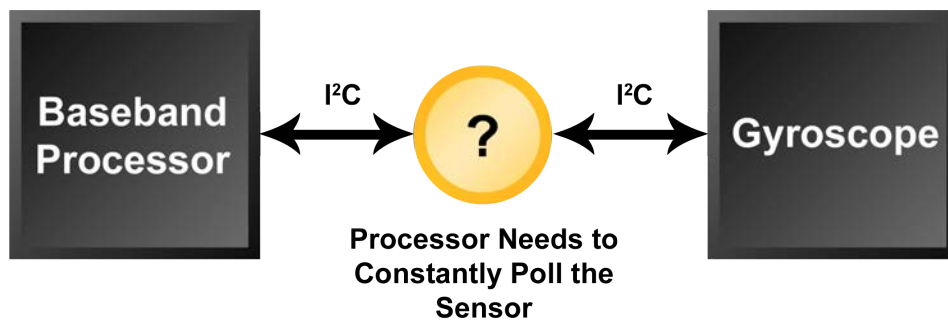
Some "chatty sensors", such as gyroscopes, require constant polling from the processor.

This is very troublesome for the processor and often prevents the processor from entering into the sleep state.

Offload processor with built-in auto-polling and data filtering

Ultra-Low Density FPGA

High Speed Parallel Bus

MSM8255/PXA920

IRQ

Processor Interface ↔ FIFO ↔ I²C Master with Auto Polling ←I²C← Gyroscope

Data Filtering
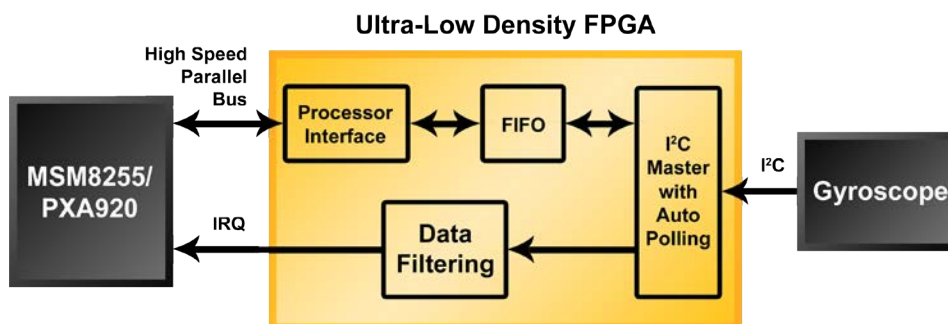
Lattice ultra-low density FPGAs can incorporate auto-polling as a feature to offload the processor.

It can further be used to filter out unnecessary data to increase interrupt efficiency.

Sensor Expansion and Management via SLIMbus
(SLIMbus to Multiple I^{2}C Interfaces)

Increasing sensors, but no good way to connect to processor

Too many sensors?

Application Processor   ?
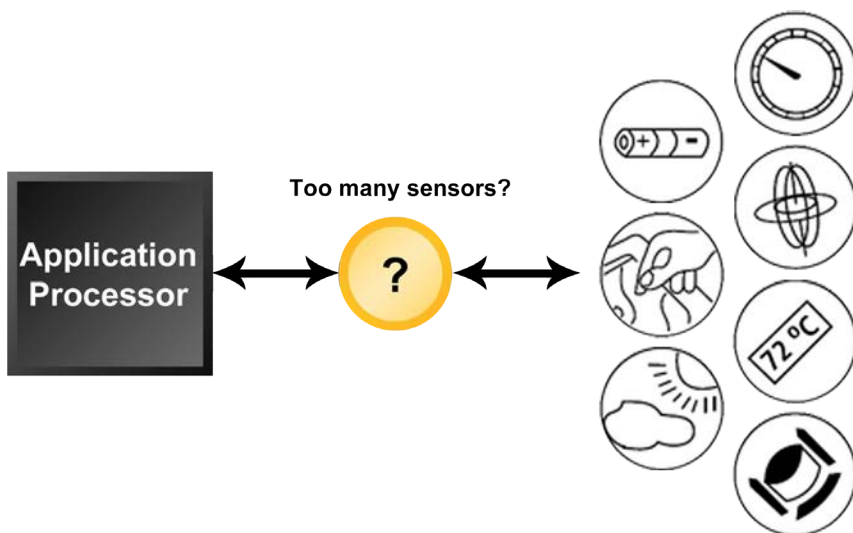
Smartphones have increasing demand for sensors.

Most of these use slow I^{2}C interfaces.

This creates an application processor I^{2}C bottleneck.

Connect multiple sensors through MIPI-SLIMbus

Ultra-Low Density FPGA

OMAP4430/PXA920 — SLIMbus — PHY Layer — Frame Layer — Message Protocol — Interface Device — I^{2}C Master #0 — I^{2}C Master #0 — Transport Protocol — Function Device — GPIO Expansion — GPIO Device
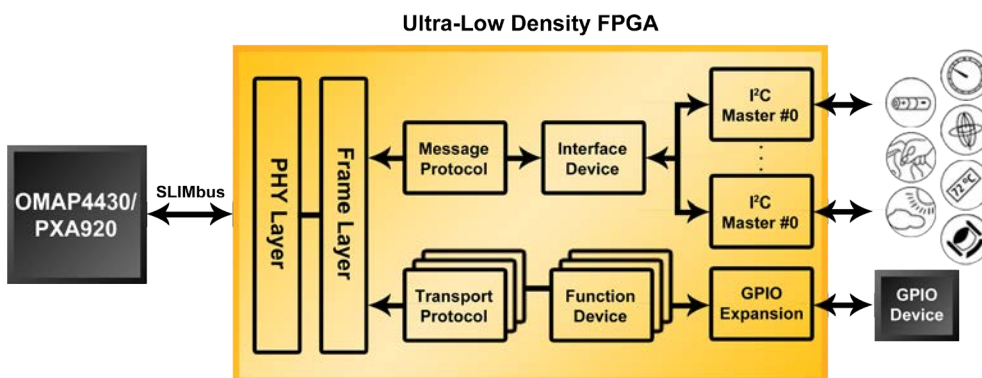
Lattice ultra-low density FPGAs can implement a SLIMbus to multiple I^{2}C adapters.

This allows the application processor to use the SLIMbus to manage the sensors.

Increasing SPI Performance to Allow Additional SPI Peripherals (SPI Port Expansion)

Many SPI peripherals on single port
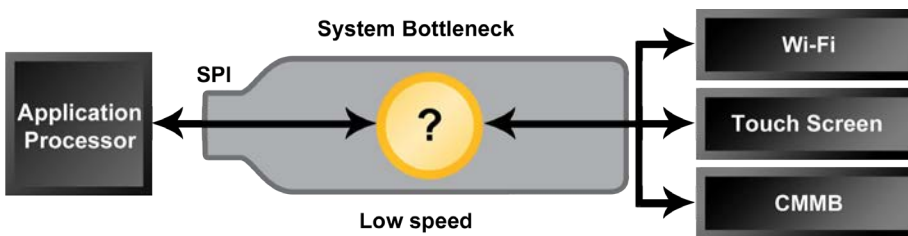
Adding additional SPI based peripherals can enrich your product.

But what if the SPI port doesn't have enough performance?

SPI port expansion
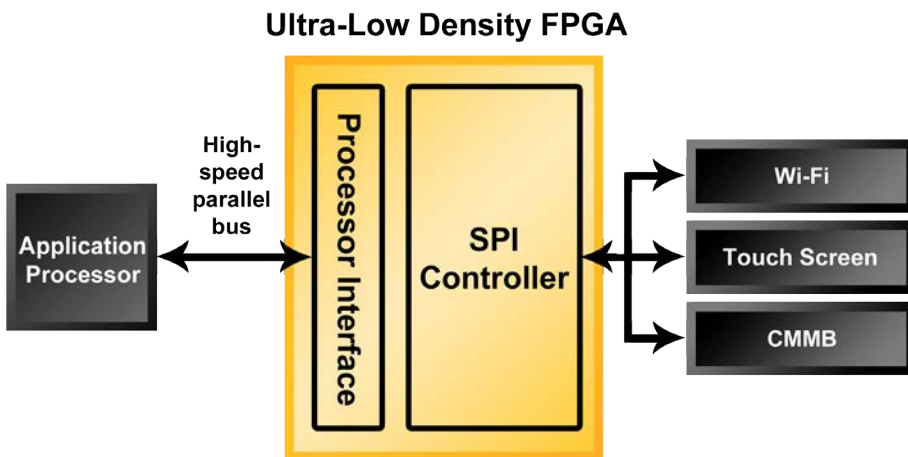
Lattice ultra-low density FPGAs can implement a high-speed SPI controller and interface it to your application processor's high-speed parallel bus.

Enabling "Always-On" Applications in Smartphones
(Always-On Pedometer)

Sensor Management chips are too power hungry
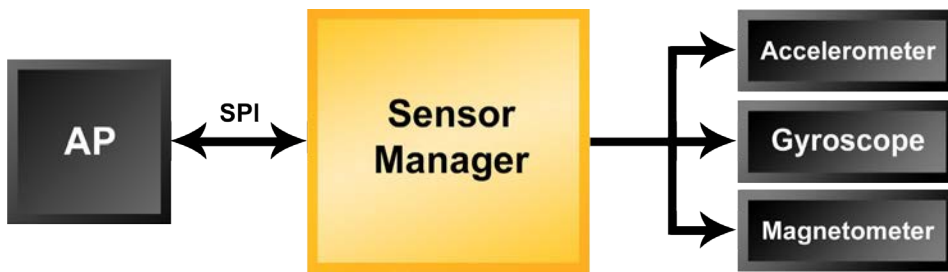
Smartphones now have several sensors.

Sensor management chips consume too much power to be used in "always on" modes - e.g. Pedometer.

Enable "Always-On" applications
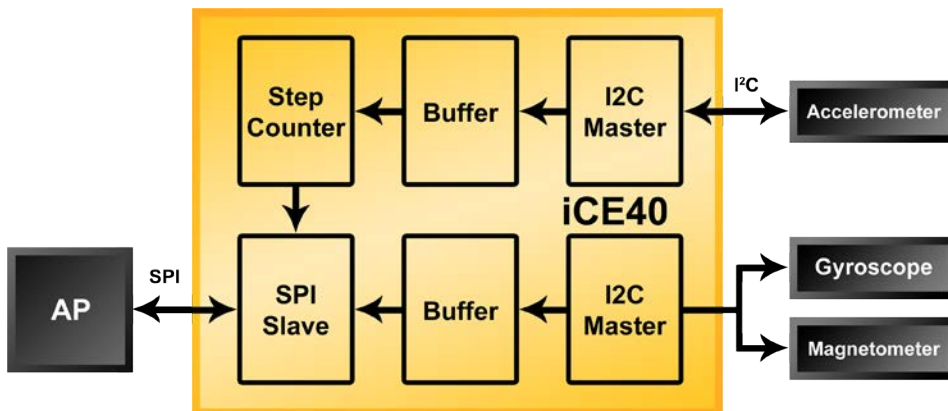
Lattice ultra-low density FPGAs can be used to create low power "always-on" solutions using the accelerometer.

Implement multiple I2C masters to completely isolate low & high power sensors.

Wake up high power sensors only after determining an event using only the low power accelerometer

Enabling Universal Remote in Smartphones
(Infrared LED Tx / Rx)

Processor can't support timing critical functions
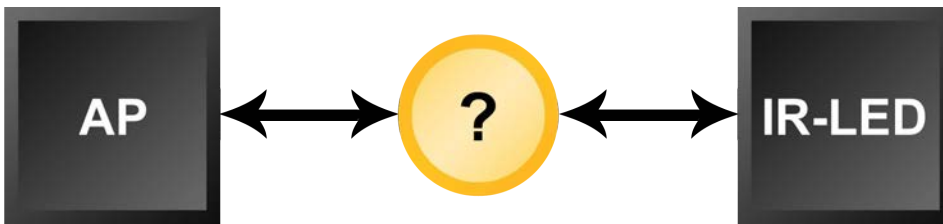
In multi-tasking operating systems, application processors need to be ready to service interrupts all the time.

This makes it challenging to manage tasks that require precision timing control.

Timing Critical Processor Offload

Ultra-Low Density FPGA
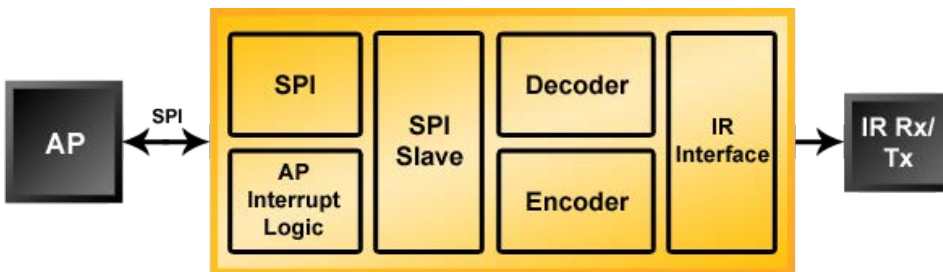
Lattice ultra-low density FPGAs can be used to offload timing critical tasks from the Application Processors.

Enabling "E-Commerce" Applications in Smartphones
(Barcode Emulation)

LCD Glass too reflective for 1-D barcode readers
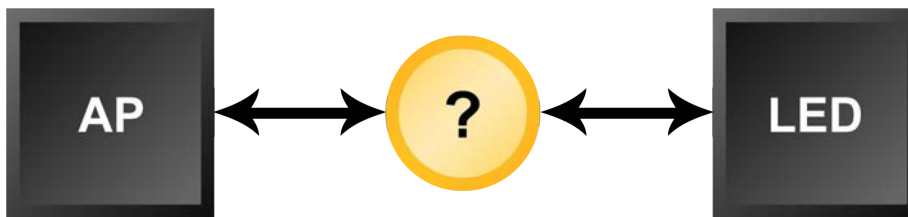
1-D barcodes displayed on the LCD screens are not readable by traditional barcode scanners

Reflections from 1-D barcodes can be emulated using a LED. This requires time critical control of LEDs.

In multi-tasking operating systems, it is not efficient for application processors to control LEDs for barcode emulation.

Timing Critical Processor Offload
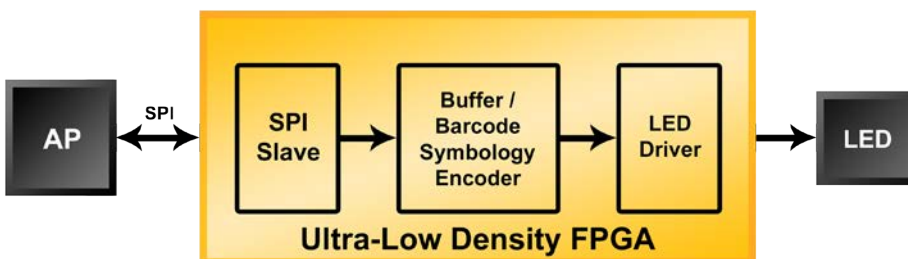
Lattice ultra-low density FPGAs can be used to offload the timing critical barcode emulation function from the application processor.

Tunable Antenna
(RFFE Bridge)

Processor can't control tunable IC within a guaranteed response time

How to guarantee the response time?

Connectivity Processor → ? → Tunable Digital Capacitor
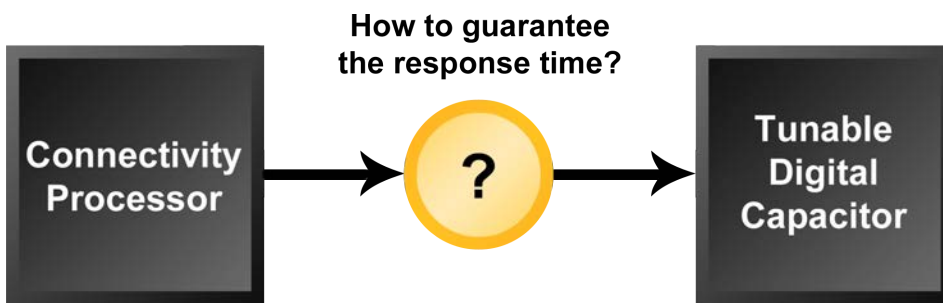
The tunable IC is controlled via the SPI interface, but the processor can't guarantee the response time through SPI interface.

Guaranteed response time with flexibility for tuning

Ultra-Low Density FPGA

MDM9200/MSM8960 —SPI→ [Tunable parameters in ROM / SPI Master] —RFFE→ Tunable Digital Capacitor

Ultra-Low Density FPGA

MDM9200/MSM8960 —RFFE→ Tunable parameters in ROM —RFFE→ Tunable Digital Capacitor
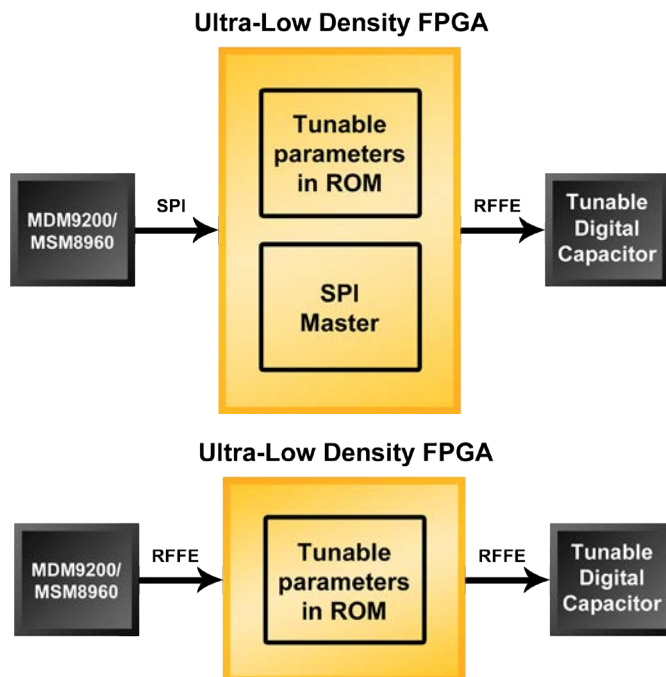
Lattice ultra-low density FPGAs can implement the needed parameters using internal block RAM for tunable IC management.

In addition, tunable parameters can be updated in the future when needed.

13

Driving High-Resolution Displays in Tablets
(Display Interface Conversion)

LVDS panel is serial (LVDS), but processor is parallel (RGB)
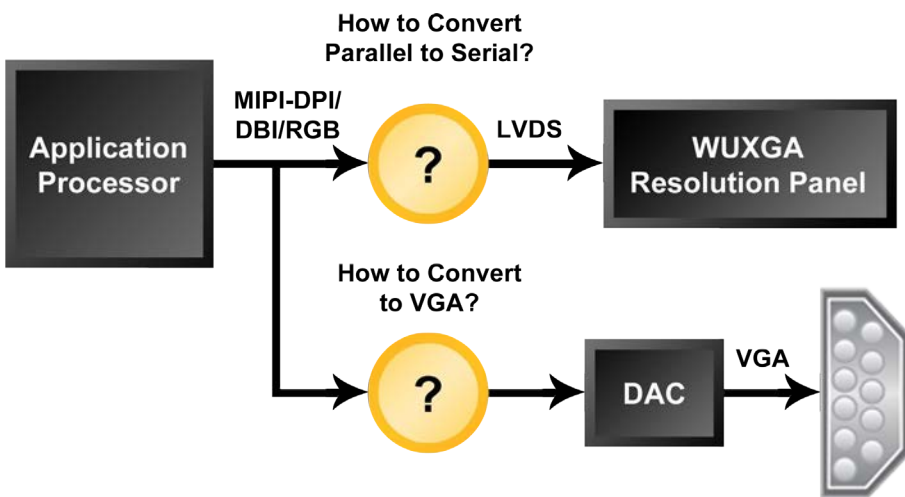
Many of the large, high-quality displays popular in today's tablets use serial LVDS inputs, while most application processors output parallel RGB video.

In addition, tablets often need to connect to external VGA displays such as projectors.

Parallel (RGB) to Serial (LVDS) conversion
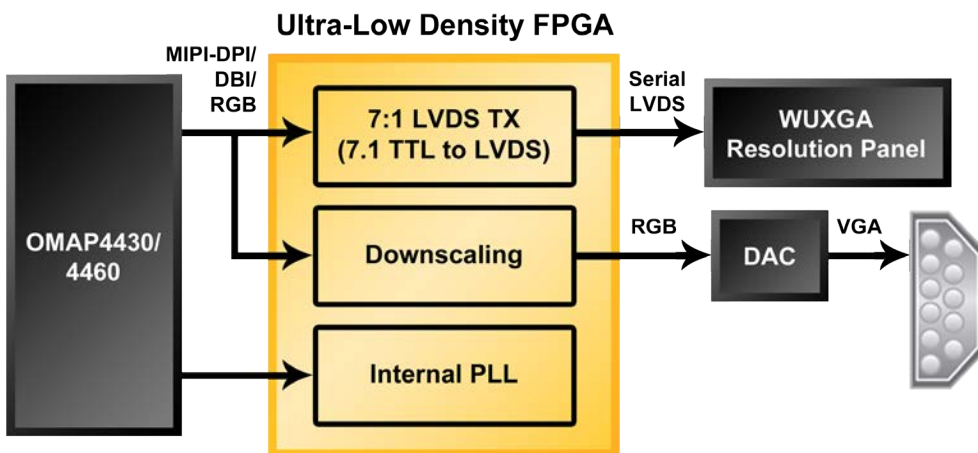
Lattice ultra-low density FPGAs can implement a 7:1 SERDES to match the application processor's parallel video output to the serial video input on the display.

In addition, the Ultra-low density FPGA can downscale the high resolution video to VGA output.

Enabling HDMI Output from Smartphones
(Video Upscaling)

Processor only supports low-resolution

Application Processor → 480p/720p → ? → 720p/1080p → HDMI Device → To External Display

How to convert
480p to 720p?
720p to 1080p?
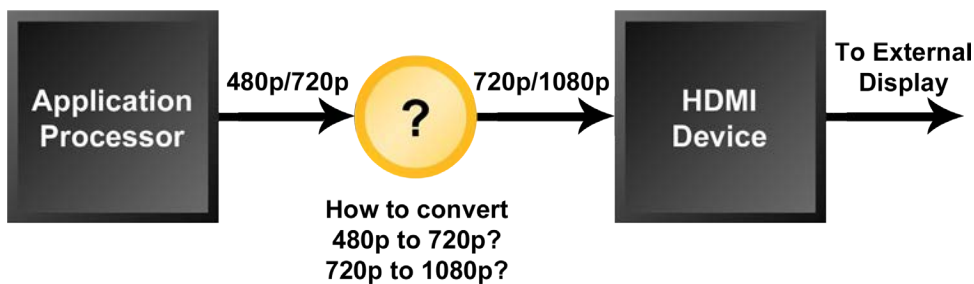
Smartphones can output 720p/1080p have a competitive advantage.

But what if application processors can only output the lower resolutions?

Upscale low resolution to high resolution

Ultra-Low Density FPGA

VM8650 → 480p/720p → Upscaler → 720p/1080p → HDMI Device → To External Display
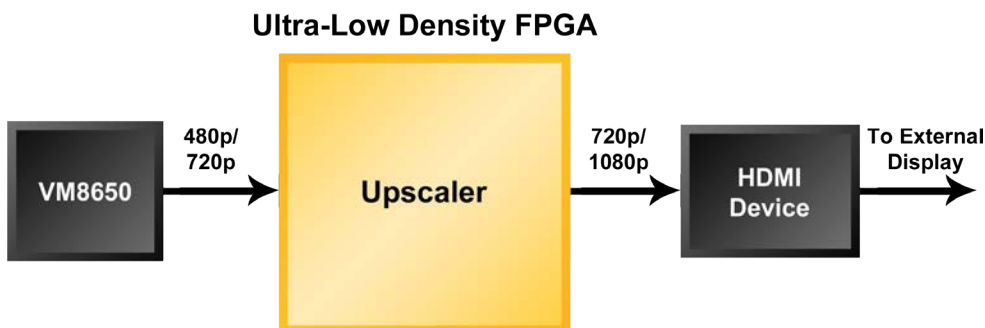
Lattice ultra-low density FPGAs can upscale the application processor's 480p/720p video output to match the HDMI 720p/1080p input.

Enabling TV Output from a Feature Phone
(Video XY Swapping)

Processor can't support Video XY swapping

Baseband Processor

Video Out

LCD (Portrait)

?

How to convert Portrait to Landscape

TV Encoder (Landscape)
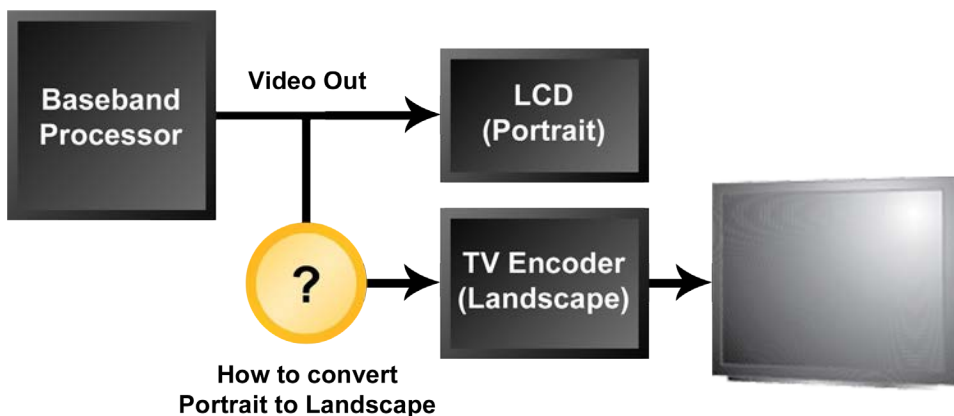
Adding an inexpensive TV encoder chip is a fast way to increase the value of your feature phone.

But most TV encoders input the image in landscape mode, while most baseband processors output the image in portrait mode.

XY swapping using an ultra-low density FPGA with external SRAM

MSM7230/ MSM7227

Video Out

LCD (Portrait)

Ultra-Low Density FPGA

TV Control

Memory Controller

TV Encoder (Landscape)
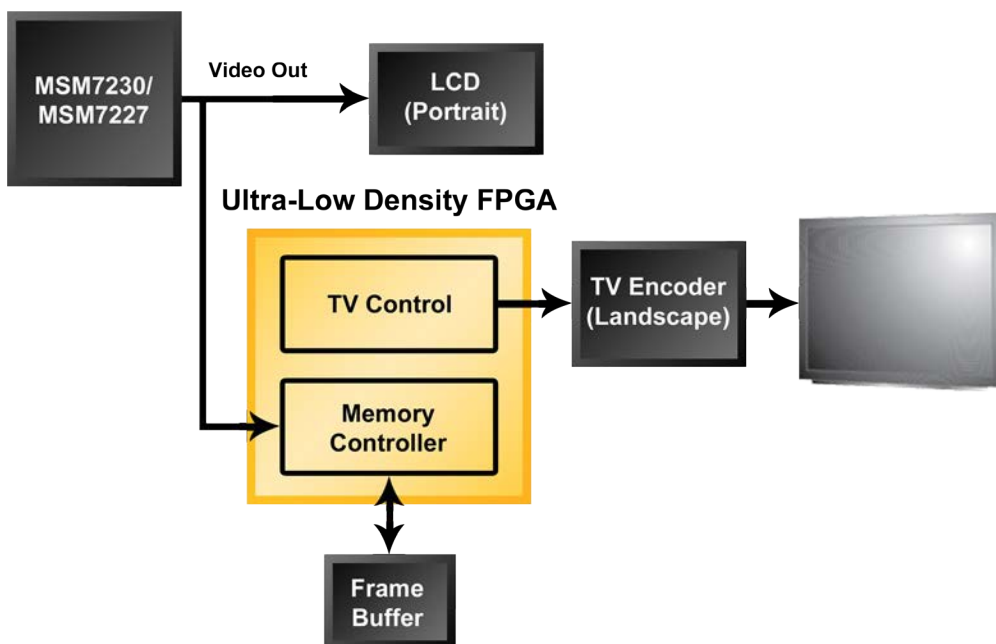
Frame Buffer

Lattice ultra-low density FPGAs can perform an video XY swap on the baseband processor's video output with an external frame buffer.

720p Wireless Video Streaming from a Smartphone
(Image Mirroring and Downscaling)

Processor does not support dual displays
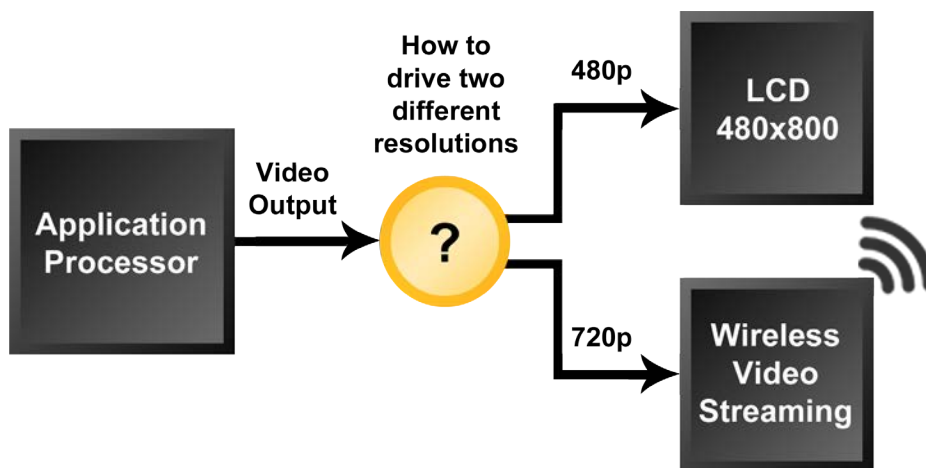
Can't connect your smartphone to your home TV.

Low-cost application processors only provide one video output. How can you drive your internal display and an external display simultaneously?

Downscale to create two resolutions
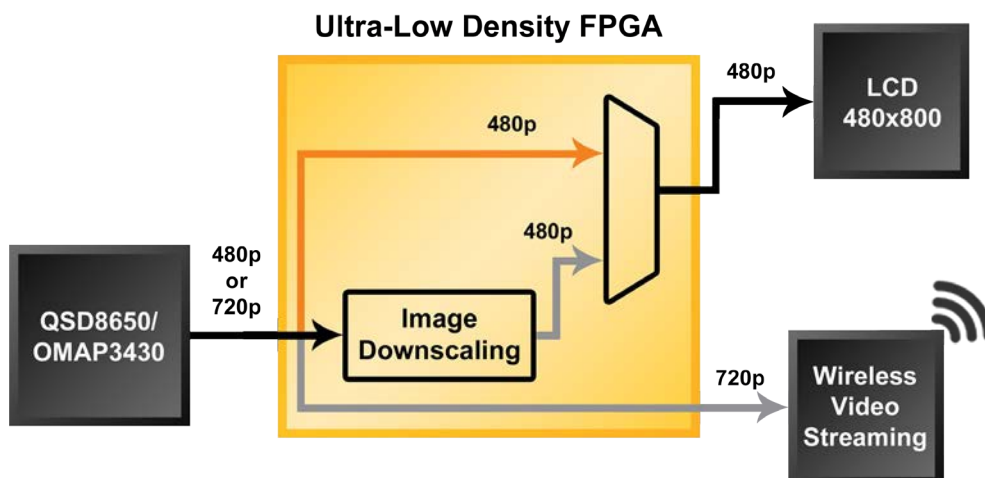
The external display's larger video resolution can be routed to a Lattice ultra-low density FPGA.

The Lattice FPGA can downscale it to match the smaller video resolution of the smartphone.

Allows both displays to be active at the same time.

3D Video and Imaging
(Autostereoscopic 3D Panel Timing Controller)

Processors can't directly drive autostereoscopic 3D panels

How to Drive 3D Panel
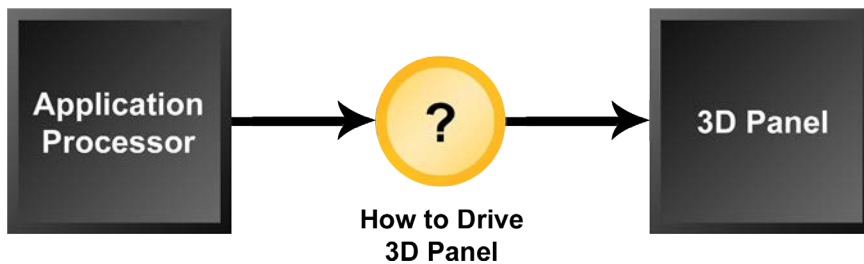
3D technology is new and there are no readily available timing controller chips to choose from.

Designers need a flexible timing controller to drive different sized displays.

Drive autostereoscopic 3D panel with built-in TCON
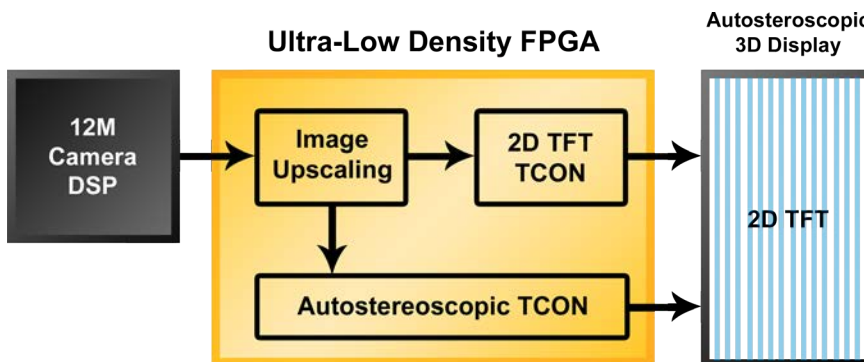
Lattice ultra-low density FPGAs implement a 3D panel timing controller and drive to a autostereoscopic.

Directly connects to a autostereoscopic 3D display for handset / mobile based products.

Universal 3D Shutter Glasses

(Customized Pattern Detector for Multiple TVs)

Different TV brands and glasses are often incompatible

Incoming IR Signals

?

It Only Works with One TV Brand
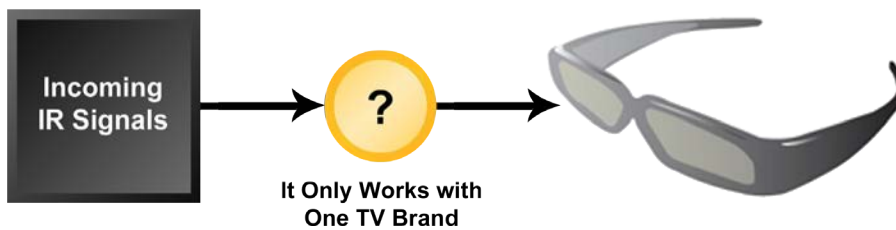
TV makers define their own IR transmission standard.

This creates incompatibility for different glasses and TVs.

Users have to abandon their glasses when changing to different TV brands.

Universal shutter glass with pre-defined pattern detection

Ultra-Low Density FPGA

Incoming IR Signals → **Noise Filtering** → **Pattern Detection Circuit (LG, Samsung, Sony, etc.)** → **SYNC Select & Shutter SYNC Generator**

Enable

LCD_Right

LCD_Left

DC-DC
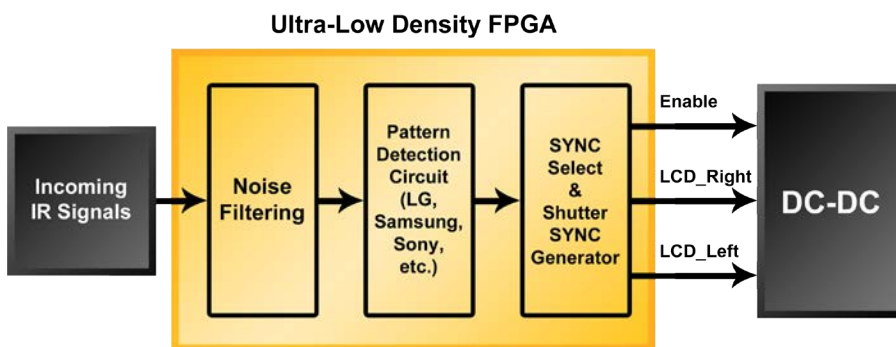
Lattice ultra-low density FPGAs can implement pattern detection circuits with preloaded patterns to support major TV brands.

In addition, IR noise filtering can be added to offer better quality viewing experience.

Managing Differing Video Requirements for Tablets
(Color Space Conversion and Timing Controller)

Processor can't convert color space

How to Color Space Convert?

YCbCr Source

?

RGB Device

?

How to Provide the Device Timing?
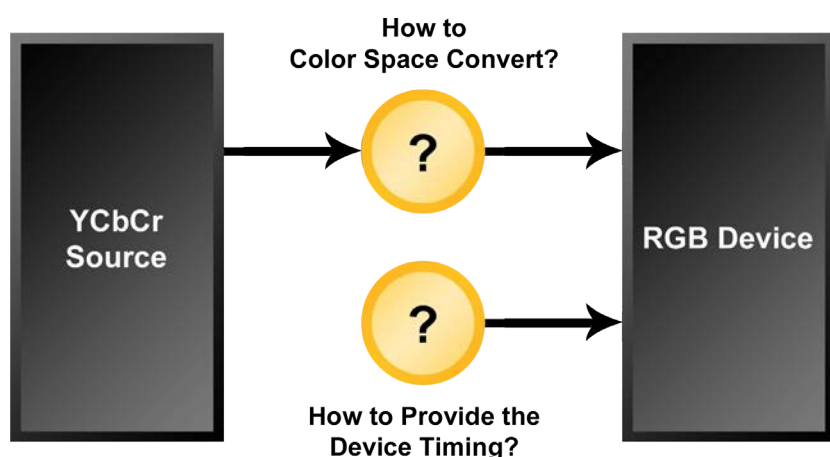
Successful tablets must be able to receive video input from multiple sources and display it on multiple devices.

However, this can be challenging for many application processors.

Use an ultra-low density FPGA for color space conversion and display timing control

Ultra-Low Density FPGA

YCbCr Source

Converter — **RGB** →

Timing Controller — **Control** →

RGB Device
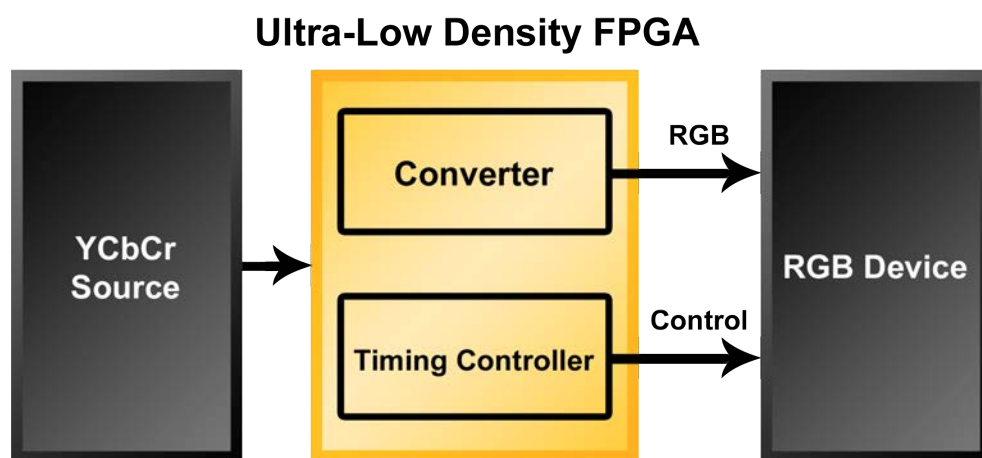
Lattice ultra-low density FPGAs can implement:
- Color Space Conversion
- Display Timing Controllers
- Image scaling

Dual Camera Video for Smartphones and Tablets
(Displaying Video-in-Video Images)

Processor lacks multi-camera support

How to Convert Camera Format to RGB?

Camera Format

?

RGB

?

How to Combine Two Video Streams into One?

Camera Format

?

Application Processor
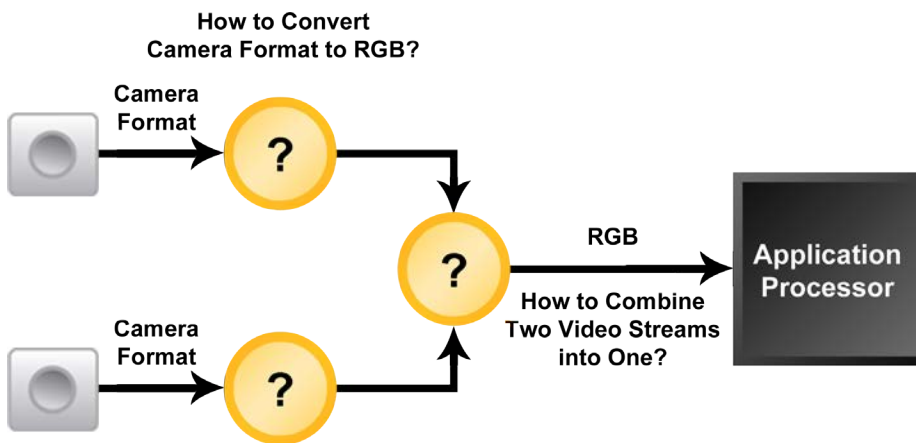
Dual cameras are becoming common in smartphones and tablets.

A popular application is to use two cameras to produce a video in video display.

Multi-camera support using an ultra-low density FPGA with external SRAM

Ultra-Low Density FPGA

Camera Format

Bayer RGB Converter /TCON 1

Camera Format

Bayer RGB Converter /TCON 2

Memory

Overlay FSM

RGB

QSD8650
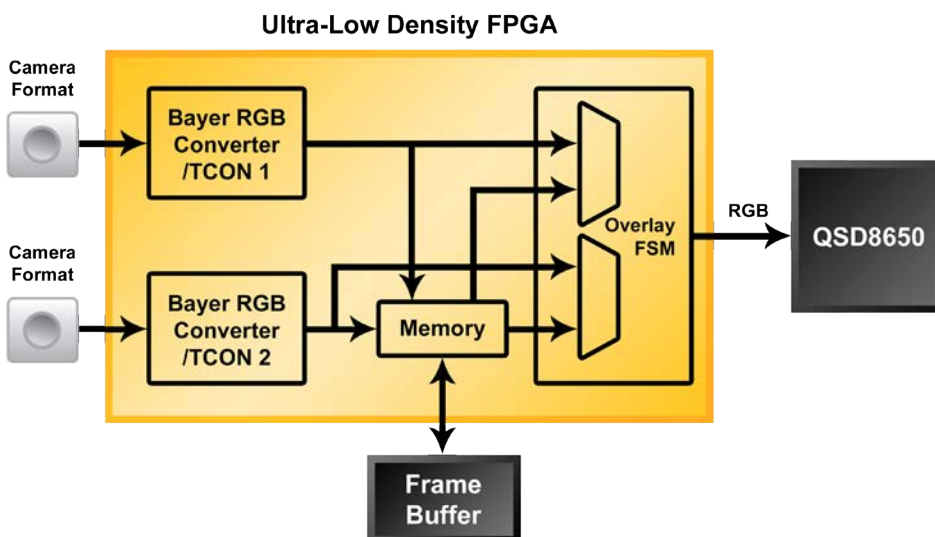
Frame Buffer

Lattice ultra-low density FPGAs can:

- Convert the camera data to RGB
- Use an external frame buffer to build the video in video image
- Interface the video image to the application processor

Enabling Dual Display Cameras
(Image Resolution Conversion)

DSPs only supports one resolution
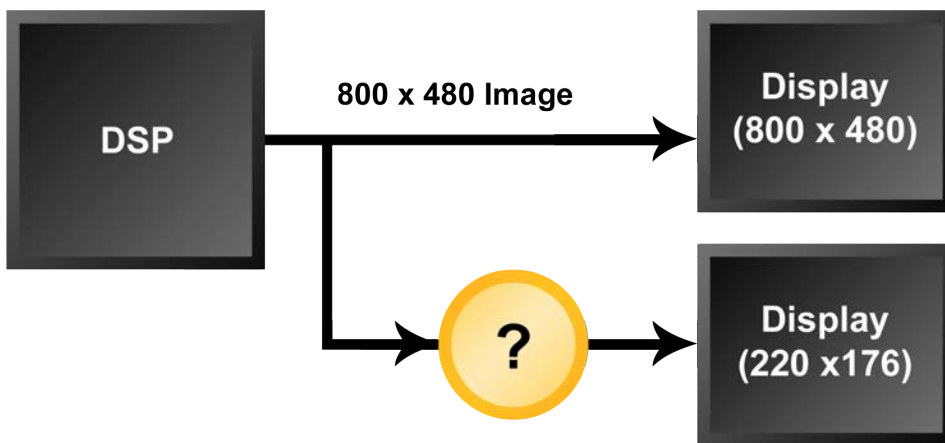
Many Imaging DSP chips have the capability to drive a display in only one resolution.

Some applications require images to be displayed in multiple LCD screens.

Downscale high resolution to low resolution
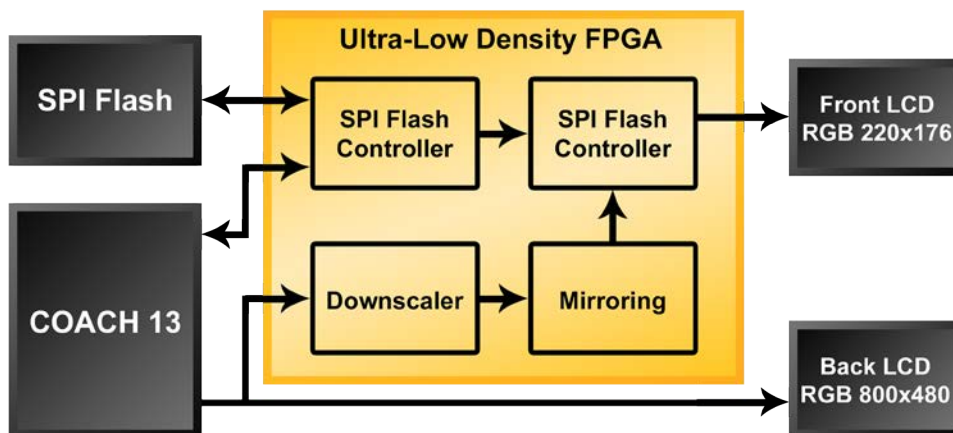
Lattice ultra-low density FPGAs can downscale the DSP's high resolution output to match the low resolution display's requirement.

Adopting Managed NAND
for Mobile Devices
(Built-in eMMC Controller)

Incompatible or lacking eMMC controller

**No dedicated
eMMC controller**

**Application
Processor**

?

**Managed
NAND**

**Wi-Fi /
DTV /
SD Memory**

SDIO port already in use
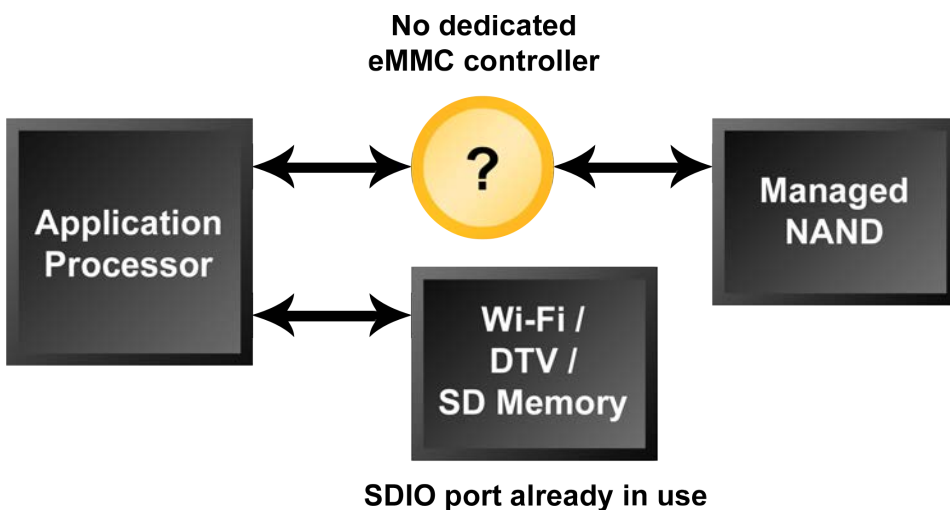
Some processors have no built-in eMMC controller, unable to take advantage of existing managed NANDs.

Many processors offer eMMC controllers through SDIO ports. However SDIO ports may already be used to connect to other peripherals.

Additional eMMC controller to lower system cost

Ultra-Low Density FPGA

**High-
speed
parallel
bus**

MSM8660

Processor Interface

**eMMC
Host
Controller**

x4 / x8

**Managed
NAND**

SDIO
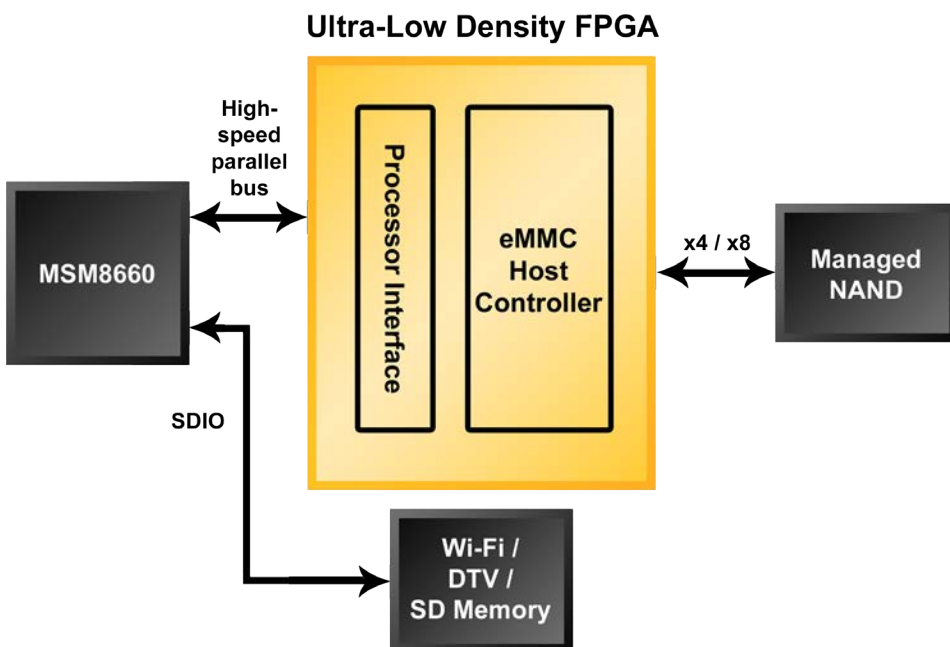
**Wi-Fi /
DTV /
SD Memory**

Implement an eMMC host controller inside a Lattice ultra-low density FPGA to take advantage of low cost managed NAND.

An eMMC controller can be customized to a x8 interface for higher performance.

23

Fast Addition of Wi-Fi or CMMB Modules

(SDIO to High-Speed Parallel Bus Bridge)

Module has two ports, but neither is free
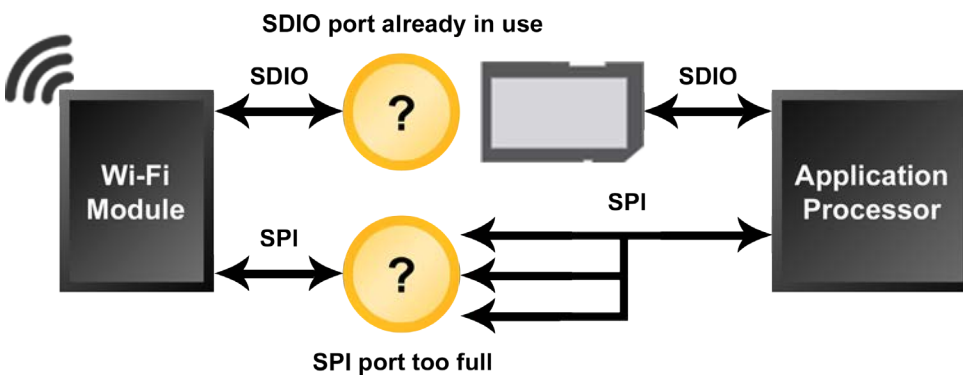
A fast way to enhance your product's feature set is to use readily available modules, such as Wi-Fi or CMMB.

Most of these modules provide SDIO and SPI interfaces.

But what if neither of these interfaces are available?

Bridge SD card to AP bus, to free up SD port for Wi-Fi module
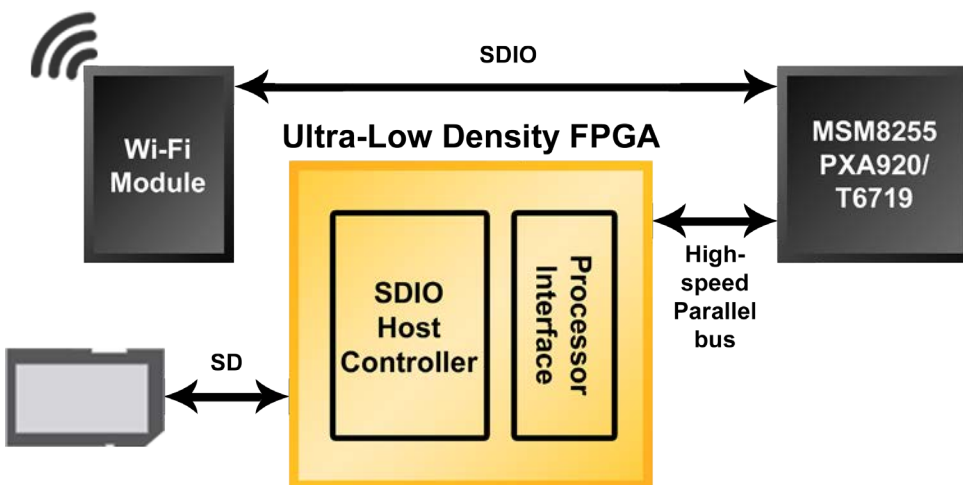
A Lattice ultra-low density FPGA can implement an SD Host Controller and bridge it to the application processor's high-speed parallel bus.

This allows the Wi-Fi module to be placed on the SD/SDIO port.

Lattice also provides reference driver code to enable rapid system integration.

Smart Frame Buffer for Notebooks

(Offloads CPU and GPU for Power Optimization)

Power consumption is high during period of inactivity

How to offload processor during period of inactivity?

GPU and CPU Subsystem → ? → Display
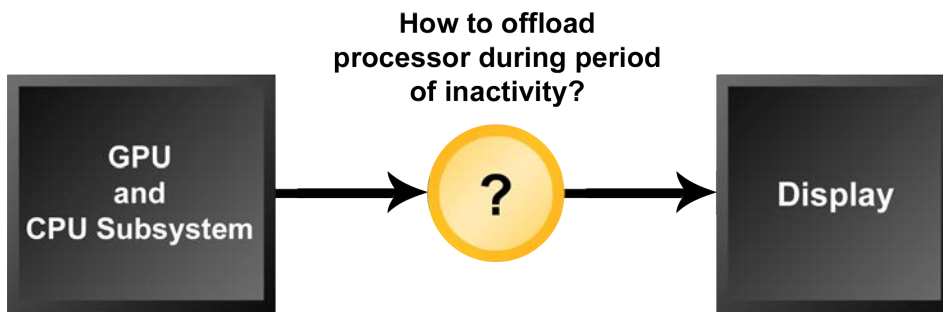
A manufacturer of ultrabooks wanted to reduce power consumption and increase battery life while still delivering the same performance of the display subsystem. The manufacturer needed a companion chip to manage the outputs of the GPU and CPU while reducing total system power.

Smart Frame Buffer offloads processor and enhances battery life

Ultra-Low Density FPGA

GPU and CPU Subsystem → PSRC Logic / LPDDR / LVDS I/F → Display
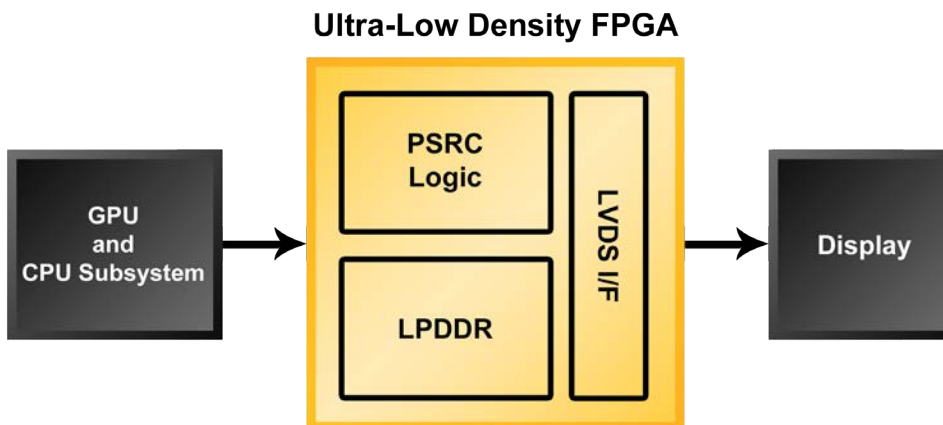
The Lattice Smart Frame Buffer ultra-low density FPGA solution enables ultrabook / notebook suppliers to increase battery life by shutting down the GPU and or CPU subsystems during periods of inactivity. The smart frame buffer manages and refreshes the display while the power-hungry CPU/GPU subsystem goes into standby.

USB Keyboard Docking for Tablets

(Full Keyboard Docking Solutions)

Designers are searching for Low-cost, flexible keyboard docking

How would a tablet connect to a keyboard and touchpad?
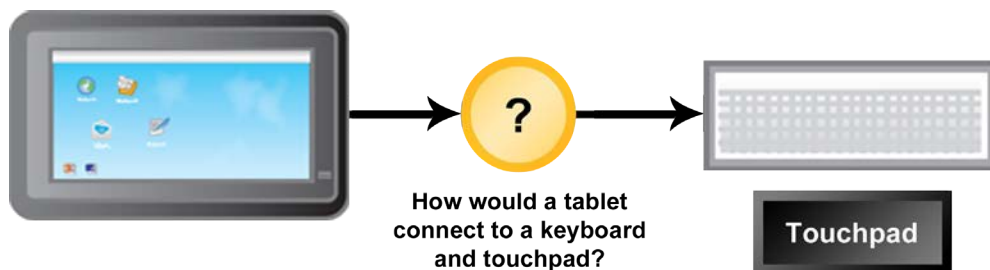
Consumers are demanding a keyboard docking station for tablets offering a notebook-like feel.

Must be low-cost, low-power and customizable.

Implement low-cost, flexible keyboard docking with an ultra-low density FPGA

Ultra-Low Density FPGA
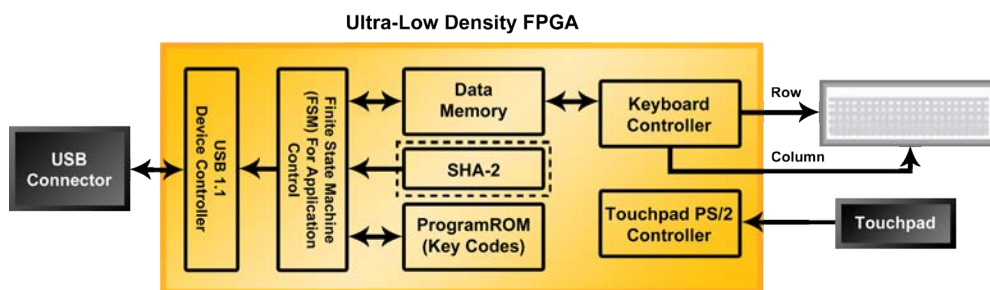
Lattice ultra-low density FPGAs are ideal for low-cost, low-power, flexible docking solutions.

Based on the USB1.1 interface, Program ROM for the keyboard can be customized to fit designer needs.

Optional touchpad and security algorithm can be implemented to offer extra authentication features and flexibility.

Media Docking for Smartphones

(Image Upscaling and Audio Muxing)

Two audio sources must share one speaker and upscaling one

How to combine radio and smartphone into decent media docking with video capability?

480p → 720p

Can it output the resolution that meets the latest standards?
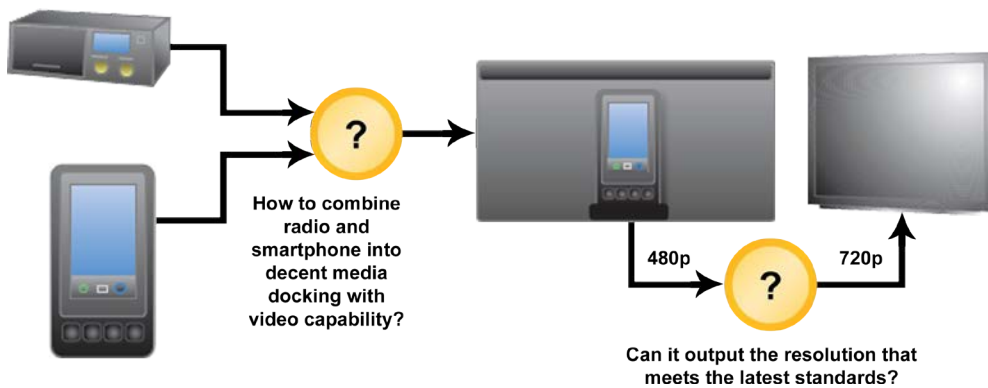
The speaker is shared between built-in radio and smartphone audio output.

Need to output 720p to TV, but the phone only offers 480p.

Muxing multiple audio sources and upscale to HDMI

Ultra-Low Density FPGA

I²S

I²S

I²C

480p

Audio Muxing

SHA-2

Video Downscaling /Upscaling

720p

Built-in Speaker

Audio Jack

HDMI Chipset
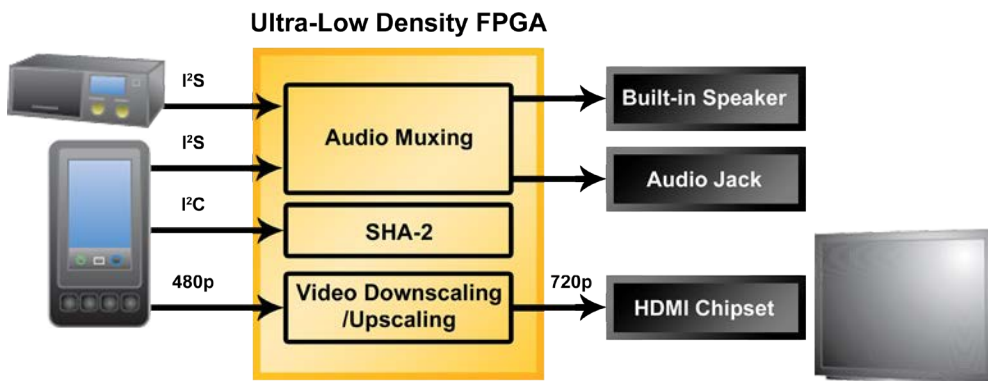
Lattice's media docking solution provides an easy way to connect all the audio and video sources from the media devices (radio/ smartphone/tablet) to the external world.

The video scaling portion of the design takes video input source from the media device; upscales it and then sends to the external HDMI connector.

In addition, authentication security algorithms, such as SHA-2 can be implemented to guarantee use of vendor-approved parts.

4G LTE Expansion for Tablets
(Additional USB2.0 Host Controller for LTE Modem)

Processor lacks USB host for LTE modem connection

Processor Does Not Offer Enough USB Host Controllers
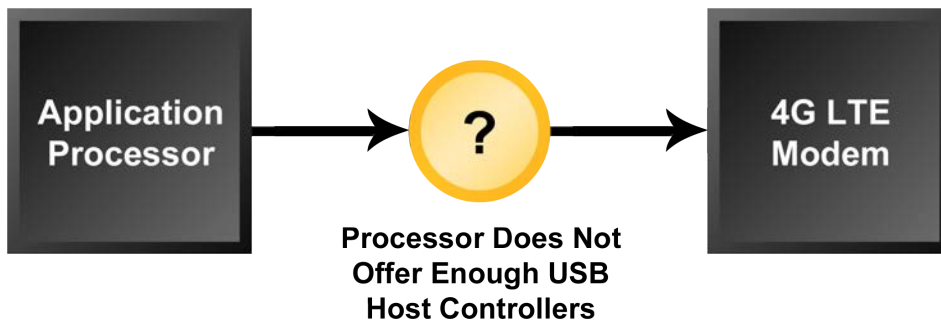
Processor's native USB host controllers are already occupied.

Need additional USB host controller to support latest 4G LTE modem.

Must guarantee 4G bandwidth of 100 Mbps downlink and 50 Mbps uplink.

USB2.0 host controller for LTE connectivity
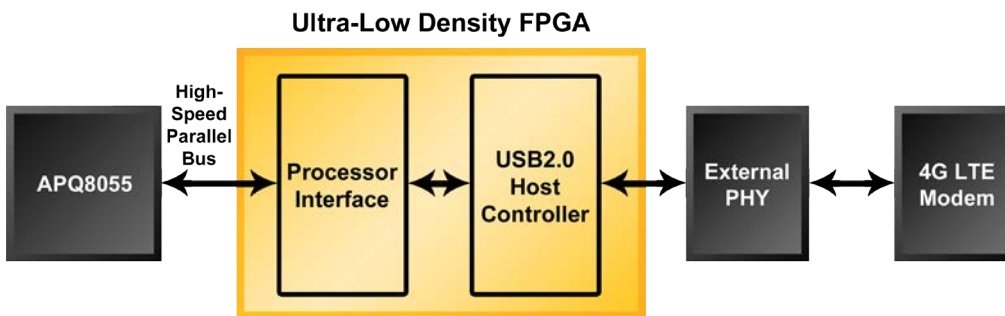
Lattice ultra-low density FPGAs can implement a USB2.0 host controller with high-speed processor interface to connect to a LTE modem.

The processor interface can be customized to be either a 16-bit or 32-bit bus to boost performance.

In addition, a DMA engine can be added to give even higher bandwidth.

Adding High-End Headsets to Smartphones
(Nokia ECI Implementation)

Processor does not support high-end audio feature

How to Interface to High End Headsets?

Application Processor → **?** →
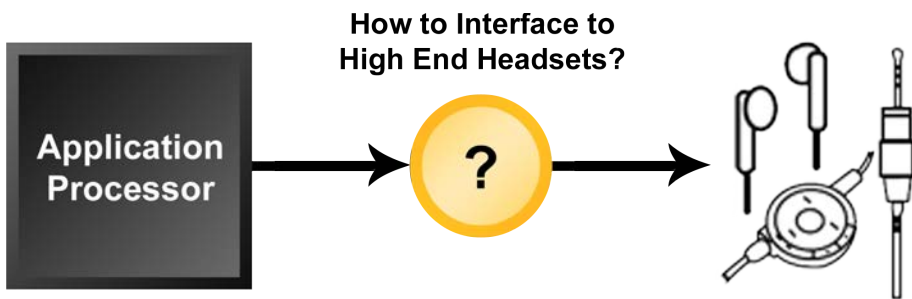
One role of smartphones is to function as a media player.

Most media players interface to a high end headset, which includes media control functions.

How can this capability be added to a smartphone?

Implement Nokia's proprietary ECI for superior audio experience

L/R Audio

OMAP4430/ MSM8660/ U8500

Processor Interface

ECI Master

REF1

REF2

2.5mm Audio Jack

Ultra-Low Density FPGA
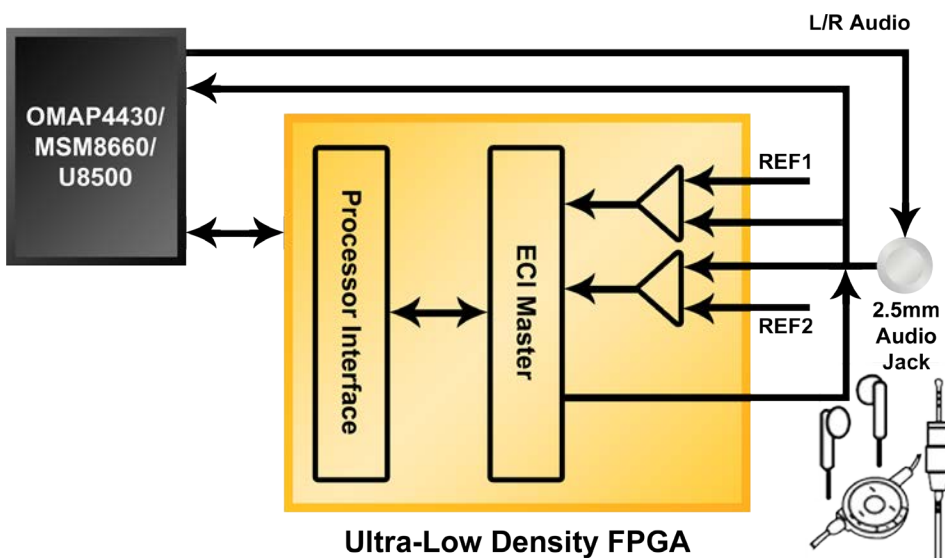
A Lattice ultra-low density FPGA to implement Nokia's ECI.

Nokia's Enhanced Control Interface (ECI) is similar to Apple's Earphones with remote and microphone.

This lets smartphone designers quickly add a high-end audio device interface.

Dual SIM Phones
(Inter-processor Communication)

How to allow inter-processor communication
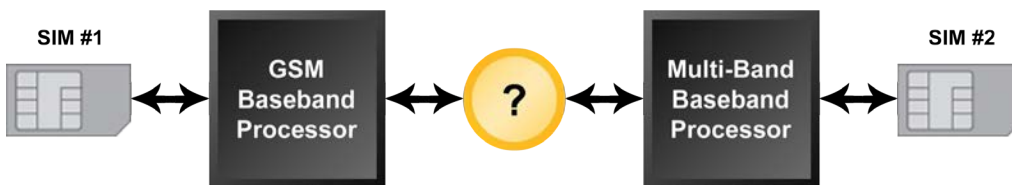
One way to implement a dual SIM phone is by using two baseband processors.

How can the two processors communicate with each other?

Create an Inter-Processor Communication Unit (IPCU)
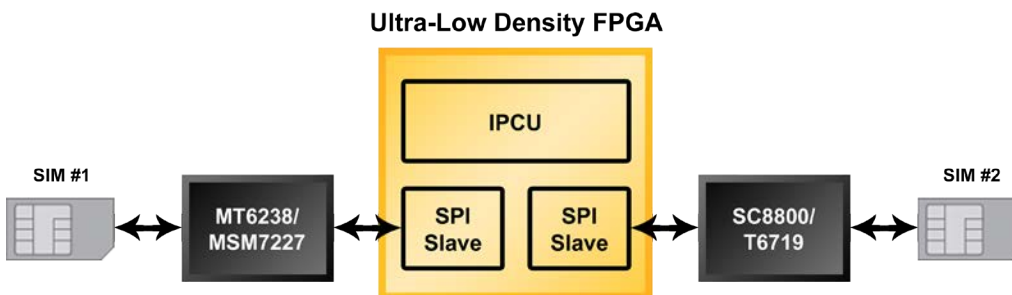
Lattice ultra-low density FPGAs can use any available port on either processor for implementing the inter-processor communication unit (IPCU).

Example interfaces for two processor using a pair of SPI slaves.

Dual SIM Phones
(SIM Card Switching)

Single baseband can't support two SIM cards

SIM #1

SIM #2

Baseband Processor

?
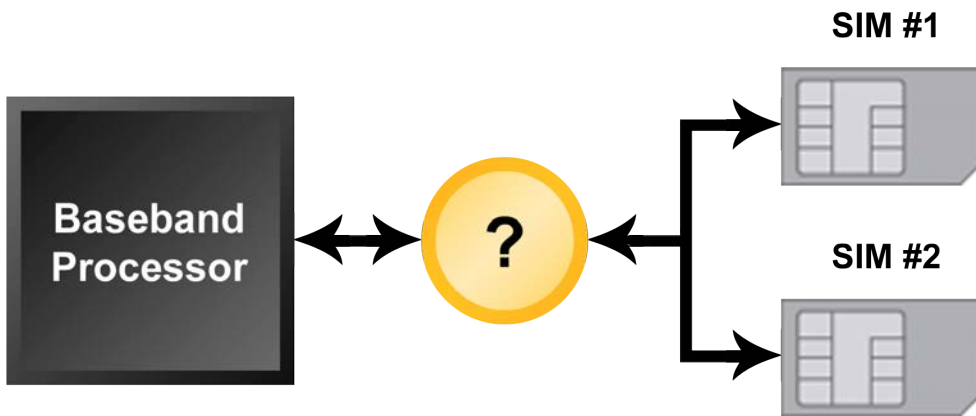
Often dual SIM phones are implemented with a single baseband processor. SIM switching logic is required to make it happen.

Implement SIM switching logic to enable dual SIM application

Ultra-Low Density FPGA

SIM #1

SIM #2

Baseband Processor

Sim Switching Logic
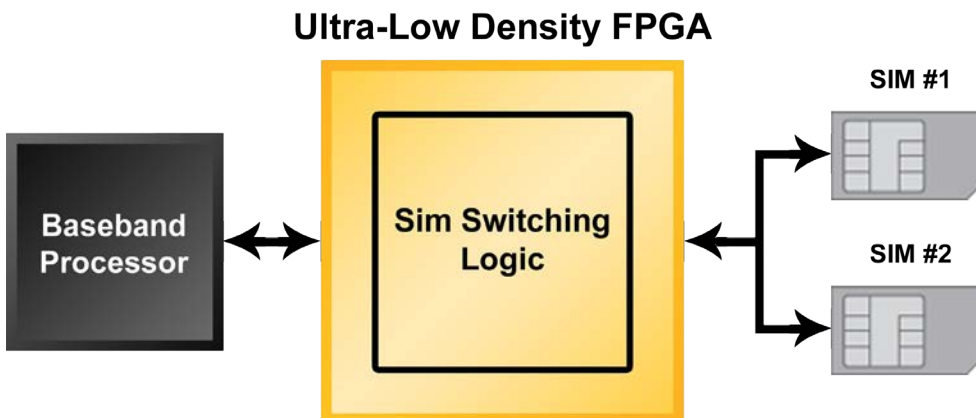
Lattice ultra-low density FPGAs can implement the SIM switching logic allowing one baseband processor to support two SIM interfaces.

High-End Camera Phone with Camera DSP Module

(Multiple Hosts Sharing Same Client)

One client, but two hosts

Application Processor

SD host & Other interfaces

Inter-processor Communication?

SD host & Other interfaces

Camera DSP

Resource sharing between two processors
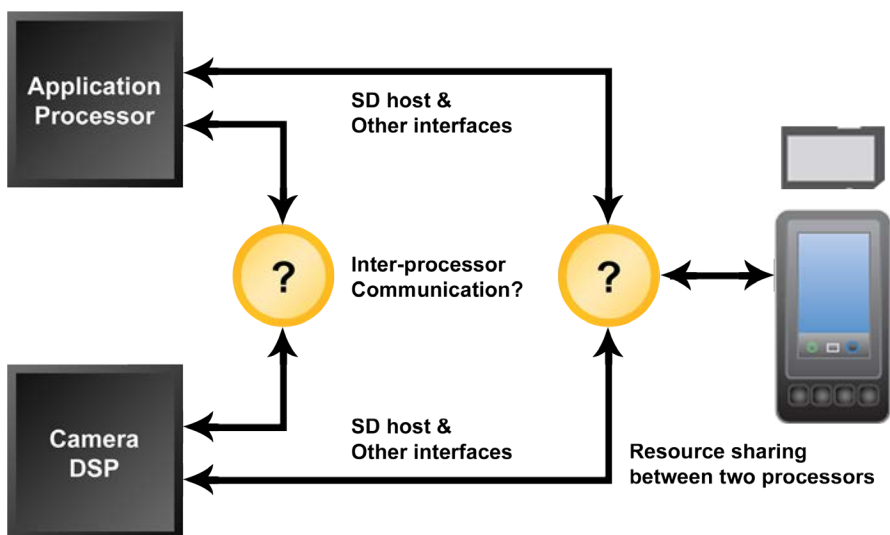
A high-end camera phone can be built by using an actual camera DSP module.

How does the camera DSP communicate with the application processor?

How do two SD hosts share one SD client?

How are other resources shared between two processors? (e.g . LCD, buttons and touch.)

Mux single client between two hosts

SD host & other interfaces **Ultra-Low Density FPGA**

MSM7227

Inter-processor Communication

μSD

LCD

Touch Screen

Buttons

12M CameraDSP

SD host & other interfaces
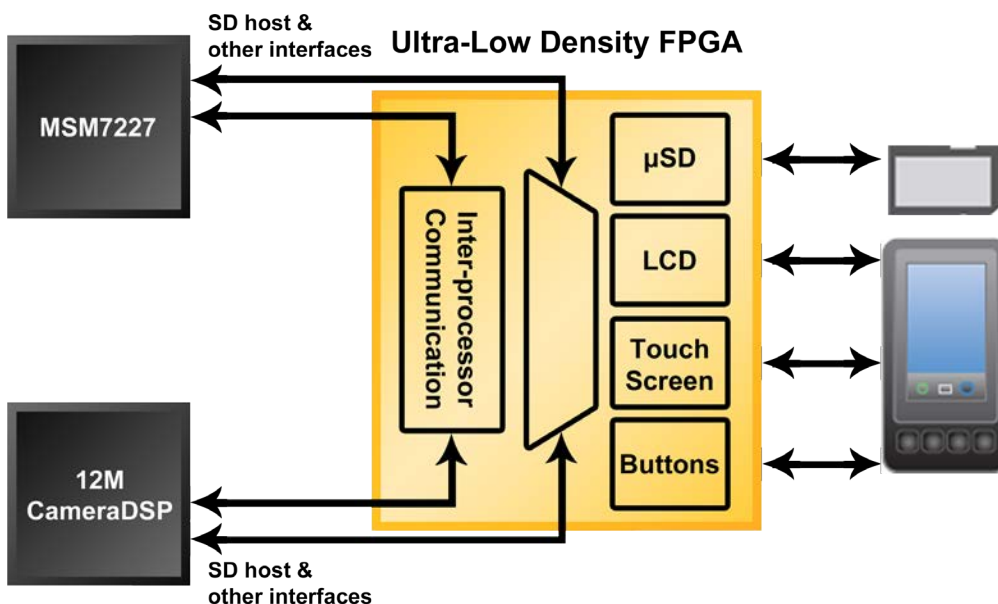
Lattice ultra-low density FPGAs can implement the necessary flags, registers, etc. to enable the inter-processor communication.

In addition, a, ultra-low density FPGA can be used to mux the single resources between two hosts.

Adding High-end Features to Low Cost Phones

(UART Expansion via the SPI Port)

Processor lacks UART ports

Too few UART ports

Baseband Processor — ? — UART Device 1 / UART Device 2 / UART Device 3
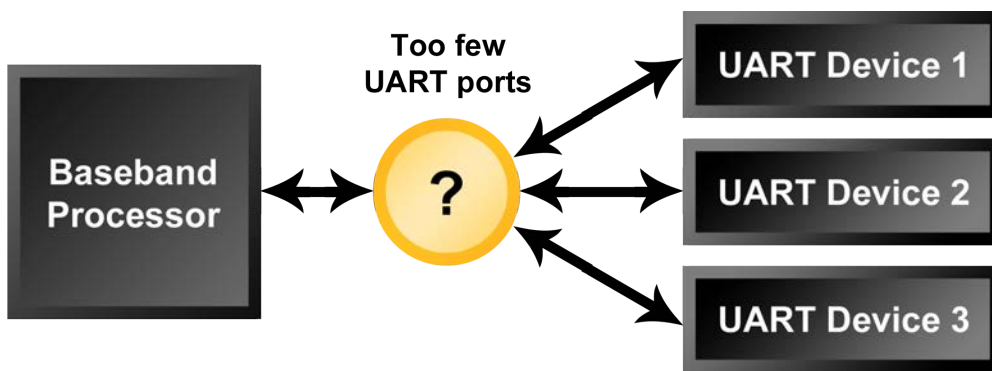
Adding additional features to a low-cost feature phone can make a big impact on your market share.

But the application processors in low cost phones usually have limited interfacing capacity.

UART port expansion through an ultra-low density FPGA

Ultra-Low Density FPGA

QSD8650/ BCM2153/ U8500 — SPI Master — SPI Slave — UART #1 / UART #2 / UART #3 — UART Device 1 / UART Device 2 / UART Device 3
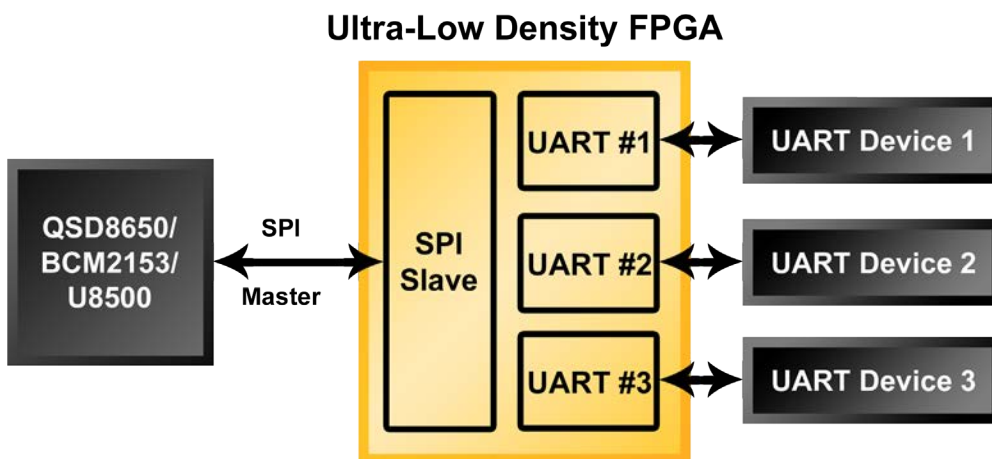
Lattice ultra-low density FPGAs can implement multiple UART controllers and interface them to the application processor's high-speed SPI port.

SLIMbus to I²S

Processor to peripherals interface mismatch

Interface Mismatch

Baseband Processor — **SLIMbus** — **?** — **No SLIMbus** — Audio Codec
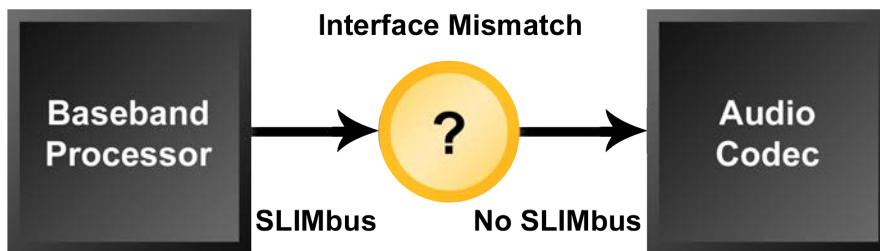
Processors have implemented SLIMbus to replace traditional audio interfaces like I²S inside the handset. However the audio codecs are slow in adopting the SLIMbus interface, causing an interface mismatch.

SLIMbus to I²S adapter solves the interface mismatch problem

Ultra-Low Density FPGA

MSM8960 — SLIMbus Slave — I²S — Audio Codec
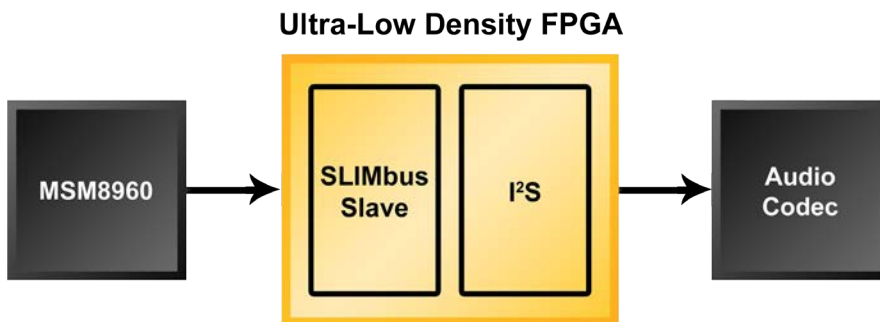
Lattice ultra-low density FPGAs can implement a SLIMbus to I²S to solve this interface mismatch problem.

Reversely, an I²S to SLIMbus host controller can be implemented to support the connectivity processor (such as MDM9200) with the SLIMbus interface to hook up to the AP supports only I²S.

MIPI-BIF (Battery Interface) for Smartphones
(Accelerates Smart Battery Adoption)

Can't connect to smart batteries using MIPI-BIF interface

How to connect?

Mobile Processor → **?** → Smart Battery
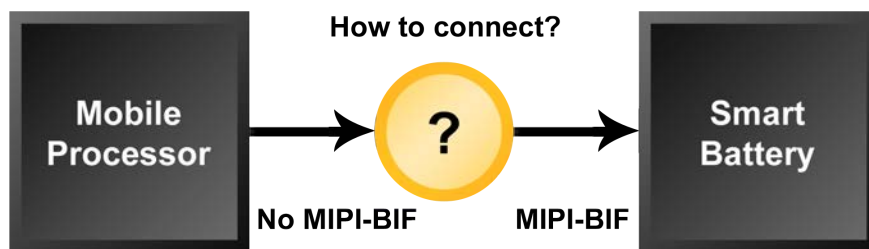
No MIPI-BIF   **MIPI-BIF**

A smart battery interface with security features can offer strong protection against the use of counterfeit batteries, providing a safer solution for end users. However, most existing mobile processors don't support the MIPI-BIF smart battery interface.

Implement MIPI-BIF for smart battery connectivity

Ultra-Low Density FPGA

MSM8960/APQ8060 → I²C or SPI Slaves | BIF Host → Smart Battery
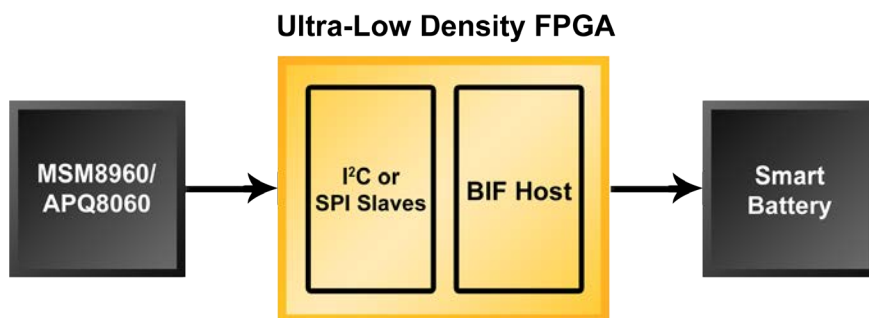
Lattice ultra-low density FPGAs can implement a complete MIPI-BIF host controller to interface to smart batteries.

This allows the mobile developer to adopting the latest battery interface standard using their existing applications processor.

Multiprocessor systems

(Custom Interface for Inter-processor Communication)

Sharing critical parameters between two processors
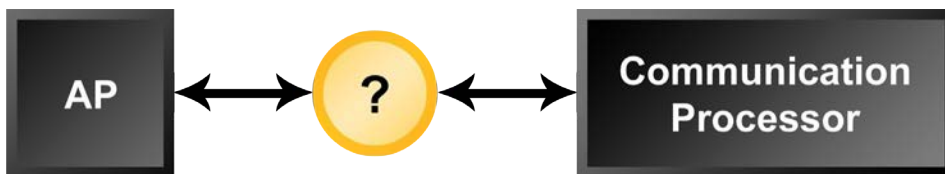
Dual port RAMs are popular in multiprocessor systems where data needs to be shared between two processors.

However, DPRAMs require high number of I/Os and are not ideal for space constrained applications.

Custom inter-processor communication unit
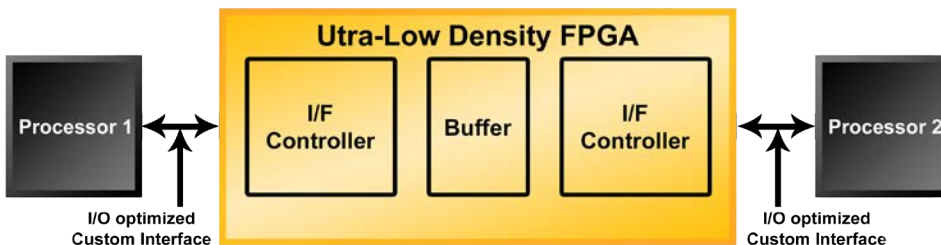
Lattice ultra-low density FPGAs can used to implement I/O optimized custom interfaces to share critical parameters between two processors.

Lattice ultra low density FPGAs are offered in several small packages that meet the requirements of space constrained applications such as Smartphones.

Mobile Application Targeted IP
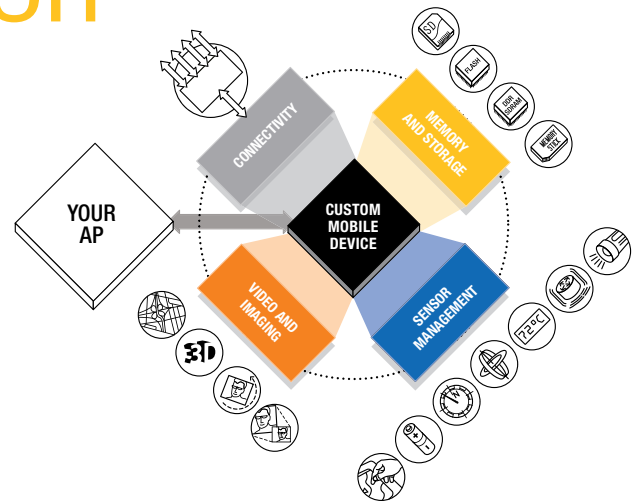
CONNECTIVITY

1-to-4 UART Expander
CMOS Camera Interface
PWM (16x3)
I²C Master / Slave Controller
SPI Master / Slave Controller
USB 2.0 Host Controller
USB 2.0 Device Controller
USB 2.0 OTG Controller
USB 2.0 Hub Controller
I²C Master / Slave Controller
PCI Master / Target Controller

SENSOR MANAGEMENT

I²C Master Controller
SPI Master Controller
SLIMbus Client Controller
UART
Expansion Memory Interface
Touchscreen Controller
PWM (16x3)
Keypad Scanner
IrDA Fast Tx/Rx

MEMORY AND STORAGE

Cellular RAM Controller
MDDR Controller
CF+Controller
MS Pro Interface
NAND Flash Interface
SLC2MLC Interface
MMC Host Controller
SD Host Controller
SDIO Host Controller
MMC Client – MMC Mode Using FPGA RAMs as Memory
SD Client – SD Mode Using NAND Flash as Memory
NOR Flash Controller
Flash Controller with Wear Leveling
LPC Bus Controller
DDR/DDR2/LPDDR Memory Controllers
SDRAM Controller

VIDEO AND IMAGING

| |
|---|
| Dual Display Controller |
| Graphics LCD Controller |
| LCD Controller (16x2 Character) |
| Touch Screen Controller |
| XGA to WVGA LANCZOS2 Scaler |
| XGA to WVGA Nearest Neighborhood Scaler |
| RGB565 to YCbCr 8bit (Color Space Conversion) |
| RGB666 to YCbCr 8bit (Color Space Conversion) |
| RGB888 to YCbCr 8bit (Color Space Conversion) |
| YCbCr 10bit to RGB666 (Color Space Conversion) |
| YCbCr 10bit to RGB888 (Color Space Conversion) |
| YCbCr 10bit to RGB565 (Color Space Conversion) |
| YCbCr 8bit to RGB565 (Color Space Conversion) |
| YCbCr 8bit to RGB888 (Color Space Conversion) |
| YCbCr 8bit to RGB666 (Color Space Conversion) |
| I²C Based Video Switching |
| Image Blending – Multiple Images and Text Overlay |
| Image Enhancements – Brightness and Contrast Controller |
| LVDS Transmitter/Receiver |
| LVDS Serializer/De-Serializer |
| DVI Receiver Controller |
| MIPI DSI Receiver / Transmitter Controller |
| MIPI CSI-2 Receiver / Transmitter Controller |
| Dual-LVDS Transmitter (after LVDS Serializer) |

OTHER

Sigma-Delta ADC
Mico8 Microcontroller
LED/OLED Driver
Power Management Bus Controller
CRC (Cyclic Redundancy Checker)
AES Encryption / Decryption
RC4-based pseudo-random sequence generator
MIPI Battery Interface (BIF)

Design Services

In addition to the Application Examples, Lattice offers a wide range of IP focusing in the areas of Sensor Management, Video and Imaging, Memory and Storage, and Connectivity. Lattice also offers custom design services.

Lattice Ultra Low Density FPGA

Design Services for Custom Chipsets

Reference Examples

Off the Shelf, Complete, Unique Designs

IP Building Blocks

Broad Selection for Building Custom Designs

CUSTOM INTERFACES

STANDARD INTERFACES

VIDEO AND IMAGING

3D IMAGING
MULTI-DISPLAY
IMAGE SCALING
LCD CONTROLLER
ROTATION
COLOR SPACE CONVERSION
VIDEO MUXING
PICTURE-IN-PICTURE

MEMORY AND STORAGE

MDDR
CELLULAR RAM
SDRAM
NAND FLASH
DUAL SIM
SD/MMC
SERIAL FLASH
CF

CUSTOM FUNCTIONS

SENSOR MANAGEMENT

AGGREGATION
ARBITRATION
PRIORITY INTERRUPT
PATTERN RECOGNITION
INTERRUPT TRAPPING
PROCESSOR OFFLOAD
POLLING
POWER OPTIMIZATION

CONNECTIVITY

I^2C
SPI
UART
SDIO
PWM
GPIO
LVDS
USB

CUSTOM INTERFACES

STANDARD INTERFACES

Device Selection Guide

Feature	iCE40							MachXO2					
	LP384	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K	256	640/U	1200/U	2000/U	4000	7000
Logic Cells	384	1280	3520	7680	1280	3520	7680	256	640	1280	2112	4320	6864
Embedded RAM Bits	0	64K	80K	128K	64K	80K	128K	0	18K/64K	64K/74K	74K/92K	92K	240K
Phase-Locked Loops	0	1	2	2	1	2	2	0	0/1	1	1/2	2	2
Core Icc @ 0KHz[1]	21µA	100µA	360µA	360µA	267µA	667µA	1100µA	18µA	28µA	56µA	80µA	124µA	189µA
Memory Standards	LPDDR							DDR / DDR2 / LPDDR					
LVDS Speed	525Mbps							756Mbps					
Package	**Programmable I/O: Max I/O (LVDS Channels)**												
25-ball WLCSP (2.5 x 2.5 mm)[5]										18			
32-pin QFN (5 x 5 mm)	21 (4)							21					
36-ball ucBGA (2.5 x 2.5 mm)	25 (3)	25 (3)[2]											
49-ball ucBGA (3 x 3 mm)	37 (6)	35 (5)											
64-ball ucBGA (4 x 4 mm)								44					
81-ball ucBGA (4 x 4 mm)	55 (3)	63 (8)	63 (9)[3]										
81-ball csBGA (5 x 5 mm)		62 (8)											
84-pin QFNS[2] (7 x 7 mm)		67 (7)											
100-pin TQFP/VQFP (14 x 14 mm)					72 (9)[2]			55	78	79	79		
121-ball ucBGA (5 x 5 mm)		95 (12)	93 (13)	93 (13)									
121-ball csBGA (6 x 6 mm)		92 (12)											
132-ball csBGA (8 x 8 mm)					95 (11)	95 (12)	95 (12)	55	79	104	104	104	
144-pin TQFP (20 x 20 mm)					96 (12)	107 (14)			107[4]	107	111	114	114
184-ball csBGA (8 x 8 mm)[6]												150	
225-ball ucBGA (7 x 7 mm)			167 (20)	178 (23)			178 (23)						
256-ball caBGA (14 x 14 mm)						206 (26)					206	206	206
256-ball ftBGA (17 x 17 mm)										206[4]	206	206	206
332-ball caBGA (17 x 17 mm)												274	278
484-ball fpBGA (23 x 23 mm)										278[4]	278	334	

1. MachXO2 (ZE option) measured at 1.2V Vcc
2. No PLL available in this package
3. Only 1 PLL available
4. Ultra high I/O count devices are supported for XO2-HC/HE options
5. WLCSP package available for ZE option only
6. Contact Lattice sales representative regarding this package, available for HE option only
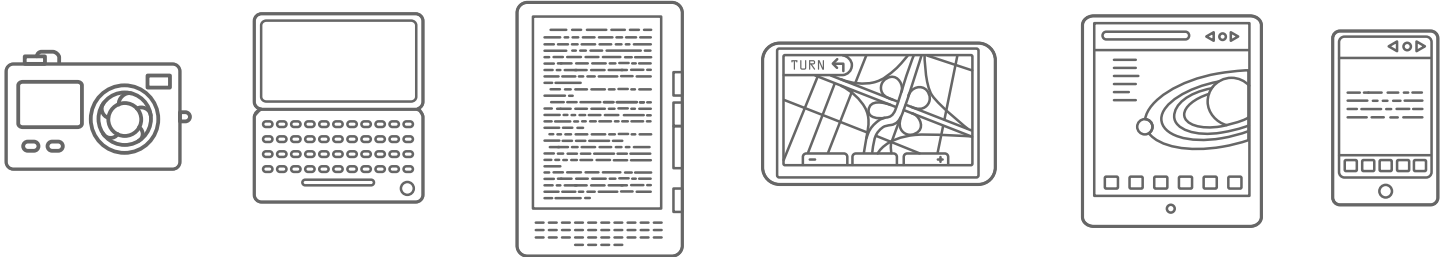
Packages Designed for Mobile Applications

iCE40 Packages

84 QFNS
0.5 mm pitch
7X7 mm

225 ucBGA
0.4 mm pitch
7X7 mm

121 csBGA
0.5 mm pitch
6X6 mm

81 csBGA
0.5 mm pitch
5X5 mm

32 QFN
0.5 mm pitch
5X5 mm

121 ucBGA
0.4 mm pitch
5X5 mm

81 ucBGA
0.4 mm pitch
4X4 mm

49 ucBGA
0.4 mm pitch
3 X 3 mm

36 ucBGA
0.4 mm pitch
2.5 X 2.5 mm

484 fpBGA
1.0 mm pitch
23x23 mm

144 TQFP
0.5 mm pitch
20x20 mm

100 VQFP
0.5 mm pitch
14x14 mm

256 caBGA
0.8 mm pitch
14x14 mm

132 csBGA
0.5 mm pitch
8x8 mm

225 ucBGA
0.4 mm pitch
7X7 mm

MachXO2 Packages

25 WLSCP
.4 mm pitch
2.5x2.5 mm

64 ucBGA
.4 mm pitch
4x4 mm

32 QFN
.5 mm pitch
5x5 mm

132 csBGA
.5 mm pitch
8x8 mm

100 TQFP
.5 mm pitch
14x14 mm

256 caBGA
.8 mm pitch
14x14 mm

256 ftBGA
1.0 mm pitch
17x17 mm

332 caBGA
.8 mm pitch
17x17 mm

144 TQFP
.5 mm pitch
20x20 mm

484 fpBGA
1.0 mm pitch
23x23 mm

Corporate Headquarters
Lattice Semiconductor Corporation
5555 Northeast Moore Court
Hillsboro, Oregon 97124-6421 USA
Telephone: +1-503-268-8000
Facsimile: +1-503-268-8347
Web: http://www.latticesemi.com

Software Licensing
Email: lic_admn@latticesemi.com
Web: http://www.latticesemi.com/licensing/index.cfm

Technical Support
USA & Canada: 1-800-LATTICE (528-8423)
For other locations: +1-503-268-8001
PLD Technical and Software: techsupport@latticesemi.com
Mixed Signal: ispPACs@latticesemi.com

Additionally, customers can receive technical support for Lattice's
Programmable Logic Products from our Asia based applications group,
by contacting Lattice Asia applications during the hours of 8:30 a.m.
to 5:30 p.m. Beijing Time (CST) +0800 UTC (Chinese and English
language only).
Asia: +86-21-52989090
techsupport-asia@latticesemi.com

October 2013
Order #: I0222F

LATTICESEMI.COM