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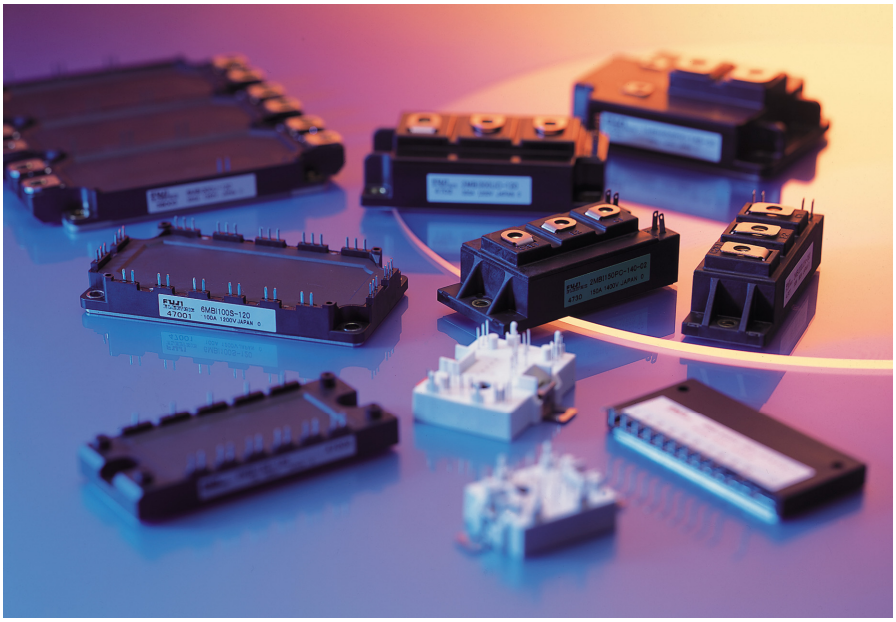
FUJI IGBT MODULES APPLICATION MANUAL



Fuji Electric Co., Ltd.

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Chapter 1

Structure and Features

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PREFACE

The insulated gate bipolar transistors (IGBTs), applied to devices such as variable-speed motor controls and uninterruptible power supplies (UPSs), widely used in response to the increasing demand for energy saving, weight saving, and downsizing of equipments in recent years. The IGBTs are switching devices designed to have the high-speed switching performance and gate voltage control of a power MOSFET as well as the high-voltage / large-current handling capacity of a bipolar transistor.

1 History of IGBT structure

The invention of IGBT was done with additional p+layer formed on the drain side of power MOSFET to produce the (n-channel) IGBT, in which n-channel was formed when the positive voltage was applied to the gate. In this device, lower resistance can be obtained even at high current because of the conductivity modulation of the base layer.

The IGBT structure can be divided roughly into the surface gate structure and the bulk structure that constitutes the base layer. There are two types of surface gate structures. One is the planar gate structure, in which the gates are formed on the semicondoucor surface. The other is the trench gate structure, in which the trenches are ectvhed to form the vertical gates in the sillicon surface. On the other hand, the bulk structure can be called as two different type the punch-through (PT) type, in which the depletion layer expands to the collector side at off-state, and the non-punch-through (NPT) type, in which it does not reach to the collector layer.

The comparison of the n-channel IGBTs is shown in Fig. 1-1.

Fuji Electric has been providing IGBTs to the market since it commercialized them in 1988. The planar-gate punch-through IGBT was the mainstream IGBT at that time. The punch-through IGBT used the epitaxial sillicon wafer and the minority carriers were high-injected from the collector side to obtain strong conductivity to achieve the low on-state voltage drop. At the same time, the carrier lifetime control method was used because the carriers, which were high-injected into the n-base layer, had to be removed quickly for fast at turn off. The low on-state voltage and the low turnoff switching loss (Eoff) were achieved in such way.

However, when the carrier lifetime control method was used, the improvement of characteristics was limited because it was hard to obtain ideal carrier profile with this method the high –injected carrers were suppressed by this technology. In addition, the disadvantages of relatively wider on-state voltage drope process variation had been an issue when IGBTs were connected in parallel especially for high power application.

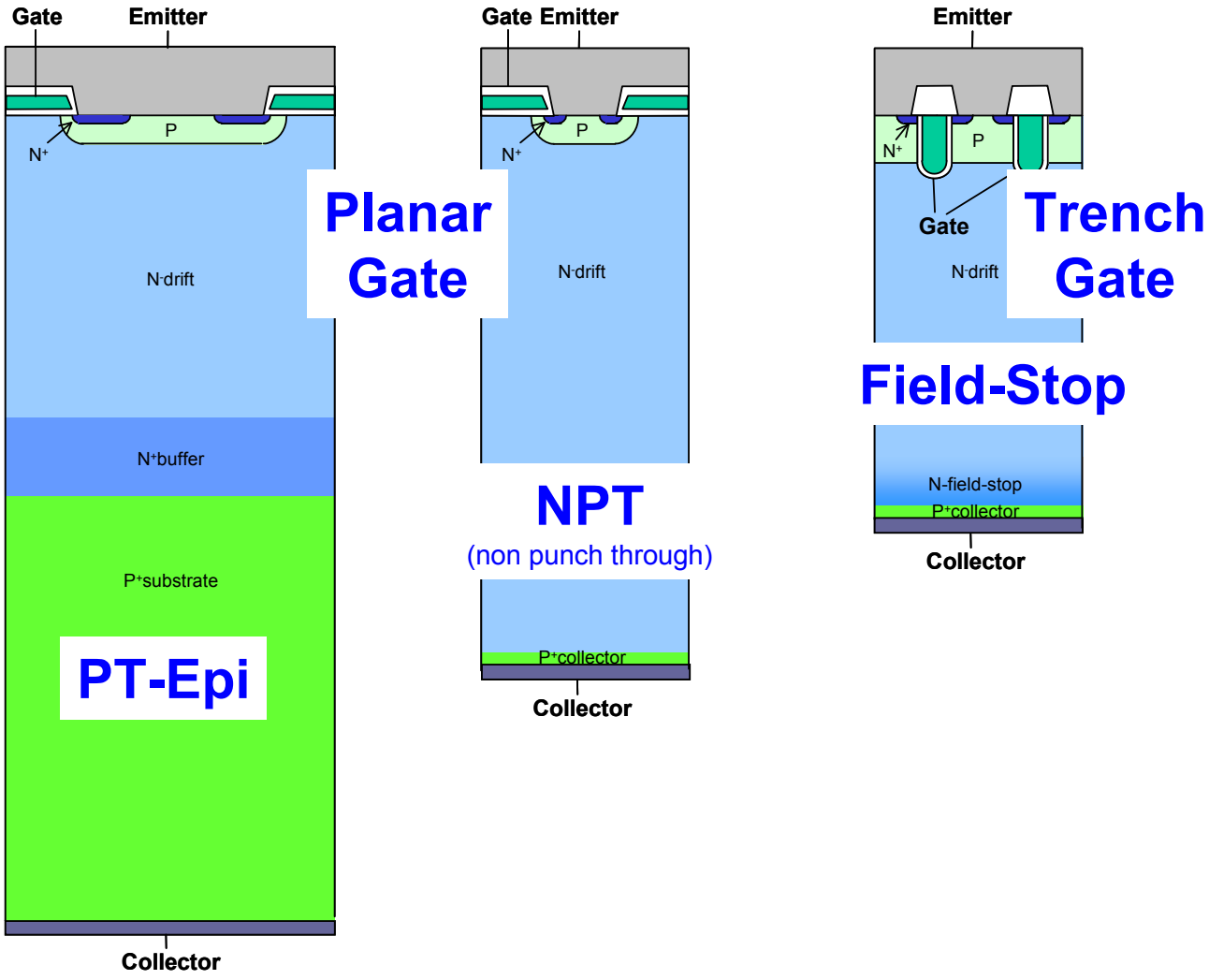
The non-punch-through (NPT) IGBT was developed to solve these issues. In NPT IGBT, the minority carrier injection efficiency of carriers was suppressed by controlling the impurity concentration in the collector (p+ layer). The transport efficiency was increased by shortening the drift distance with thinner n-base layer The NPT IGBT were fabricated the float zone (FZ) wafer instead of the epitaxial wafer, which has advantages of less crystal defects. On the other hand, it was necessary to have high transport efficiency and have the n-base layer thinner, namely make the chip thickness smaller, in order to have low on-stage voltage. Fuji Electric has developed new technologies for thinner wafers production and contributed to keep improving the IGBT performance

Thinner devices structures were necessary for additional improvement in IGBT characteristics because the thickness of the n-base layer was a major part of the chip thickness however the n-drift layer thickness is also important for the device blocking capability. It was hard to have simple thickness reduction in NPT IGBT structure while keep high performance as well as high beakdown voltage.

The field stop (FS) structure has solved this issue of improvement of the characteristics. In the FS structure, the high concentration FS layer is provided in the n-base layer, enabling additional improvement in IGBT performance.

Fuji Electric has also implemented fine pattan silicon process in surface side structures to improve the characteristics of IGBT. The IGBT chip consists of many arranged structures called “unit cells”. In general the more the IGBT cells are provided, the lower the on-state voltage will be. Therefore, the surface structure has changed from the planar structure, in which the IGBT cells are made planarly on the semicondutor surface, to the trench structure, in which the trenches are formed into the silicon to is forme three-dimensionall gate structure.

As shown, Fuji Electric has improved the characteristics by applying various technologies to the bulk structure and the surface structure.



(a) Punch Through type (b) Non Punch Through type (c) Field Stop type

Fig. 1-1 Structure comparison of IGBTs

2 Module structures

Fig.1-2 and Fig.1-3 show typical IGBT module structures. The module integrated with a terminal block shown in Fig.1-2 has a case and external electrode terminals molded into a single unit to reduce the number of parts required and cut the internal wiring inductance. In addition, the use of a direct copper bonding (DCB) substrate makes for a high-reliability product that combines low thermal resistance and high voltage isdolation.

The wire terminal connection structure module shown in Fig.1-3 has main terminals bonded to the DCB substrate by thin wires, rather than by soldering, to simplify and downsize the package structure. This results in reduction both in module height and weight, and fewer assembly person-hours.

Other design considerations implemented include an optimal IGBT and FWD chip layout to assure efficient thermal distribution and the equal arrangement of IGBT devices in the upper and lower switches to better turn-on transient current balances and thus prevent increases in turn-on energy.

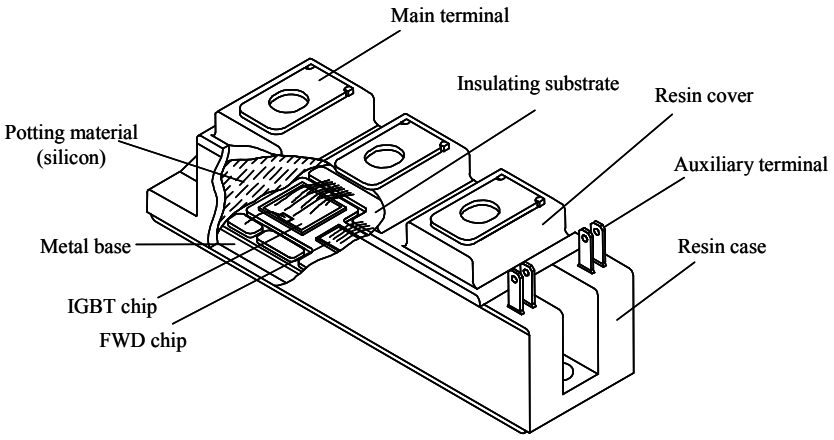


Fig. 1-2 Integrated with a terminal block type IGBT module

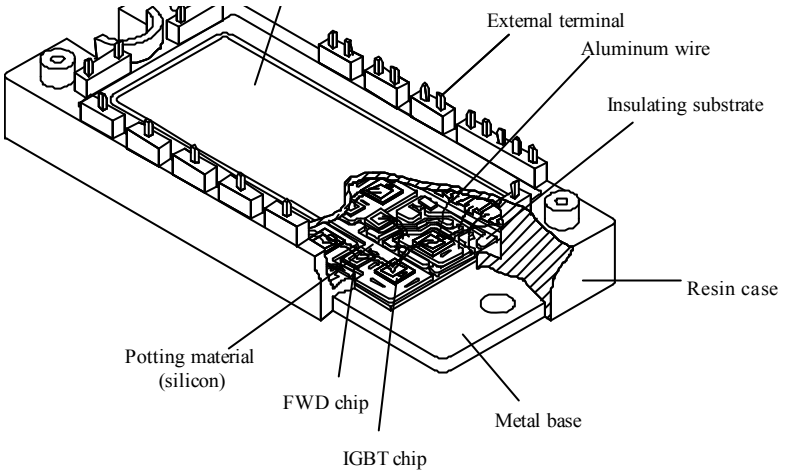


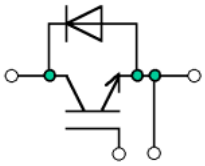
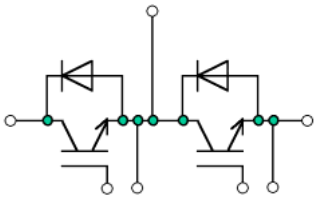
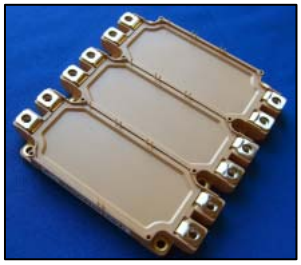
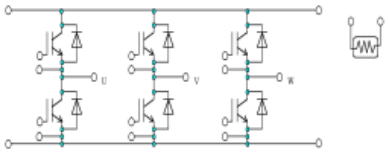
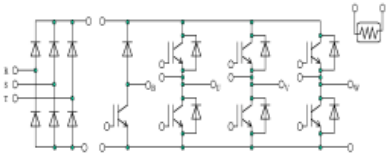
Fig. 1-3 Wire terminal connection structure type IGBT module

3 Circuit configuration of IGBT module

Table 1-1 shows typical circuit configuration of IGBT modules.

IGBT modules are configurationally grouped into four types: 1 in 1, 2 in 1, 6 in 1, and PIM (7 in 1). A circuit configuration is prescribed for each of these types. A summary description of the features of each type is also included in the figure to aid you in your device selection.

Table 1-1 Circuit configuration of IGBT modules

Type	Example of IGBT module		Features
	External view	Equivalent circuit	
1 in 1			Each product contains one switch of IGBT chip and one FWD chipset. Products having a high current rating are often connected in parallel in large capacity applications.
2 in 1			Each product contains two switchs of IGBT chips and two FWD chipset. Three units are generally used in a set to make up a 3-phase PWM inverter. Otherwise, products having a high current rating are often connected in parallel.
6 in 1			Each product contains six switches of IGBT chips and six FWD chipset. Some modules have integrated NTC. Available to congigure PWM inverter just with one module.
PIM (7 in 1)			7 in1 contains seven switches of IGBT chips and seven FWD chipset in the inverter and brake section. PIM includes a converter section in addition to 7 in1. Some types have integrated NTC.

4 Overcurrent limiting feature

During operation, a load short-circuit or similar insability may cause an overcurrent in the IGBT. If the overcurrent status keep continued, the device may quickly be overheated and results destruction. The time span from the beginning of an overcurrent to the destruction of the device, is generally called the “short-circuit withstand capability time”. The short-circuit withstand capability time depends on the conditions for ecample, it would be longer if lower short-circuit current and/or lower power supply voltage.

The IGBT module has feature of current saturation by itself to several times of the rated current This feature makes it possible to have limited over current in the event of a short circuit, which results the device a relatively high short-circuit withstand capability.

5 RoHS compliance

The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) was enacted by the EU on July 1, 2006 to restrict the use of certain hazardous substances in electrical and electronic equipment. The use of the following six substances are restricted: Pb (lead), Cd (cadmium), Cr6+ (hexavalent chrome), Hg (mercury), PBB (polybrominated biphenyl), and PBDE (polybrominated diphenyl ether). Products containing any of these hazardous substances cannot be sold in the EU.

In the IGBT module, lead (Pb) used to be contained in the solder used to connect between the respective chips and the DCB and between the base and the DCB. However, currently Fuji Electric uses the lead-free solder in compliance with RoHS.

6 Standards for Safety: UL Certification

In the areas such as North America where the UL standards are enacted, UL approval must be obtained for any part used for devices used in such areas.

In this connection, the UL approval (UL1557) is granted to the IGBT module of Fuji Electric. The approved models can be checked in following website:

http://database.ul.com/cgi-bin/XYV/template/LISEXT/1FRAME/index.htm

When “e82988” is input into the UL file number on this website for search, a list of UL-approved parts is displayed.

Chapter 2

Technical Terms and Characteristics

CONTENTS

This section explains relevant technical terms and characteristics of IGBT modules.

1 IGBT terms

Table 2-1 Maximum ratings

Term	Symbol	Definition explanation (See specifications for test conditions)
Collector-emitter voltage	V_{CES}	Maximum collector-emitter voltage with gate-emitter shorted
Gate-emitter voltage	V_{GES}	Maximum gate-emitter voltage with collector-emitter shorted
Collector current	Ic	Maximum DC collector current
	Ic pulse	Maximum pulse collector current
	-Ic	Maximum forward DC current of internal diode
	-Ic pulse	Maximum forward pulse current of internal diode
Maximum power dissipation	Pc	Maximum power dissipation per element
Junction temperature	Tj	Maximum chip temperature, at which normal operation is possible. You must not exceed this temperature in the worst condition.
Operation junction temperature	$Tj_{(op)}$	Chip temperature during continuous operation
Case temperature	T_c	Case temperature during continuous operation. Especially base plate temperature is defined.
Storage temperature	T_{stg}	Temperature range for storage or transportation, when there is no electrical load on the terminals
FWD I^2t	I^2t	Value of joule energy (value of integration of overcurrent) that can be allowed within the range which device does not destroy. The overcurrent is defined by a line frequency sine half wave (50, 60Hz) and one cycle.
FWD surge current	I_{FSM}	The maximum value of overcurrent that can be allowed in which the device is not destroyed. The overcurrent is defined by a line frequency sine half wave (50, 60Hz).
Isolation voltage	V_{iso}	Maximum effective value of the sine-wave voltage between the terminals and the heat sink, when all terminals are shorted simultaneously
Screw torque	Mounting	Maximum and recommended torque when mounting an IGBT on a heat sink with the specified screws
	Terminal	Maximum and recommended torque when connecting externals wires to the terminals with the specified screws

Caution: The maximum ratings must not be exceeded under any circumstances.

Table 2-2 Electrical characteristics

Term		Symbol	Definition explanation (See specifications for test conditions)
Static characteristics	Zero gate voltage collector current	I_{CES}	Collector current when a specific voltage is applied between the collector and emitter with the gate and emitter shorted
	Gate-emitter leakage current	I_{GES}	Gate current when a specific voltage is applied between the gate and emitter with the collector and emitter shorted
	Gate-emitter threshold voltage	$V_{GE(th)}$	Gate-emitter voltage at a specified collector current and collector-emitter voltage
	Collector-emitter saturation voltage	$V_{CE(sat)}$	Collector-emitter voltage at a specified collector current and gate-emitter voltage
	Input capacitance	C_{ies}	Gate-emitter capacitance, when a specified voltage is applied between the gate and emitter as well as between the collector and emitter, with the collector and emitter shorted in AC
	Output capacitance	C_{oes}	Gate-emitter capacitance, when a specified voltage is applied between the gate and emitter as well as between the collector and emitter, with the gate and emitter shorted in AC
	Reverse transfer capacitance	C_{res}	Collector-gate capacitance, when a specified voltage is applied between the gate and emitter, while the emitter is grounded
	Diode forward on voltage	V_F	Forward voltage when the specified forward current is applied to the internal diode
Dynamic characteristics	Turn-on time	t_{on}	The time between when the gate-emitter voltage rises from 0V at IGBT turn-on and when the collector-emitter voltage drops to 10% of the maximum value
	Rise time	t_r	The time between when the collector current rises to 10% of the maximum value at IGBT turn-on and when collector-emitter voltage drops to 10% of the maximum value
		$t_{r(i)}$	The time between when the collector current rises to 10% and when the collector current rises to 90% of the maximum value at IGBT turn-on
	Turn-off time	t_{off}	The time between when the gate-emitter voltage drops to 90% of the maximum value at IGBT turn-off and when the collector current drops to 10% of the maximum value
	Fall time	t_f	Time required for collector current to drop from 90% to 10% maximum value
	Reverse recovery time	t_{rr}	Time required for reverse recovery current in the internal diode to decay
	Reverse recovery current	$I_{rr}(I_{rp})$	Peak reverse current during reverse recovery
Reverse bias safe operating area		RBSOA	Current and voltage area when IGBT can be turned off under specified conditions
Gate resistance		R_G	Gate series resistance (See switching time test conditions for standard values)
Gate charge capacity		Q_g	Gate charge to turn on IGBT

Table 2-3 Thermal resistance characteristics

Term	Symbol	Definition explanation (See specifications for test conditions)
Thermal resistance	$R_{th(j-c)}$	Thermal resistance between the IGBT case and the chip or internal diode
	$R_{th(c-f)}$	Thermal resistance between the case and the heat sink, when the IGBT is mounted on a heat sink using the specified torque and thermal compound
Case temperature	T_c	IGBT case temperature

Table 2-1 Thermistor characteristics

Term	Symbol	Definition explanation (See specifications for test conditions)
Thermistor resistance	Resistance	Thermistor resistance at the specified temperature
B value	B	Temperature coefficient of the resistance

2 IGBT characteristics

This section illustrates the characteristics of the new 6th- generation IGBT modules, using the V series 6MBI100VB-120-50 (1200V, 100A) as an example.

2.1 Static characteristics

While the IGBT is on, the collector-emitter voltage (V_{CE}) changes in accordance with the collector current (I_C), gate voltage (V_{GE}), and temperature (T_j). The V_{CE} represents a collector-emitter voltage drop in the ON state, and is used to calculate the power dissipation loss of the IGBT. The smaller the V_{CE} value, the lower the power dissipation loss. Therefore, it is necessary to design the IGBT to have the smallest V_{CE} value possible.

The dependence of V_{CE}-V_{GE} on I_C is shown on the graph in Fig. 2-1 (T_j=25°C), and Fig. 2-2 (T_j=150°C). V_{CE} increases in direct proportion to the collector current and inversely proportional to the V_{GE} value. Note that when the Ic value is small, as T_j increases V_{CE} decreases, and when the I_C value is large, as T_j increases V_{CE} increases. Keep this in mind when determining operating conditions.

It is generally recommended to keep V_{GE} at 15V, and the collector current at the rated I_C current or lower.

Fig.2-3 shows the gate voltage V_{GE} and the collector-emitter voltage V_{CE} characteristics where the graph of Fig. 2-1 was replaced with the Ic dependency of the V_{CE} - V_{GE} characteristics.

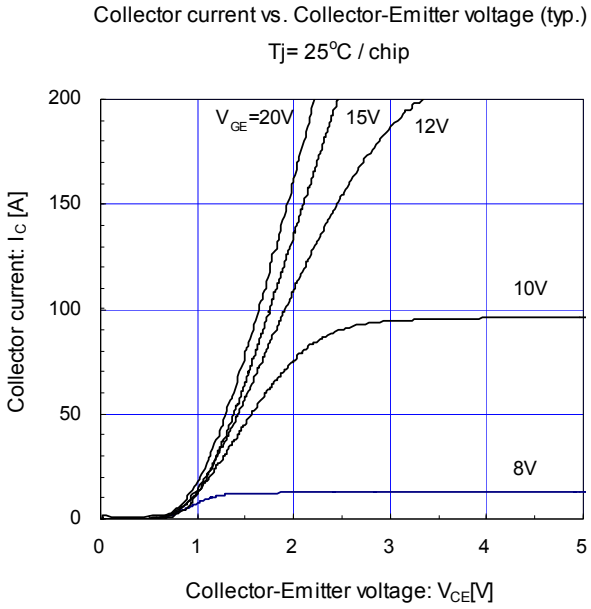


Fig. 2-1 $V_{CE(sat)}$ - I_C characteristics (Tj=25°C)

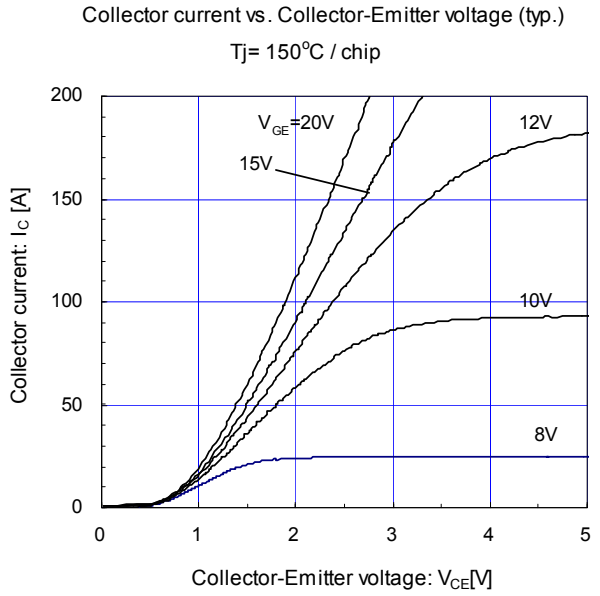


Fig. 2-2 $V_{CE(sat)}$ - I_C characteristics (Tj=150°C)

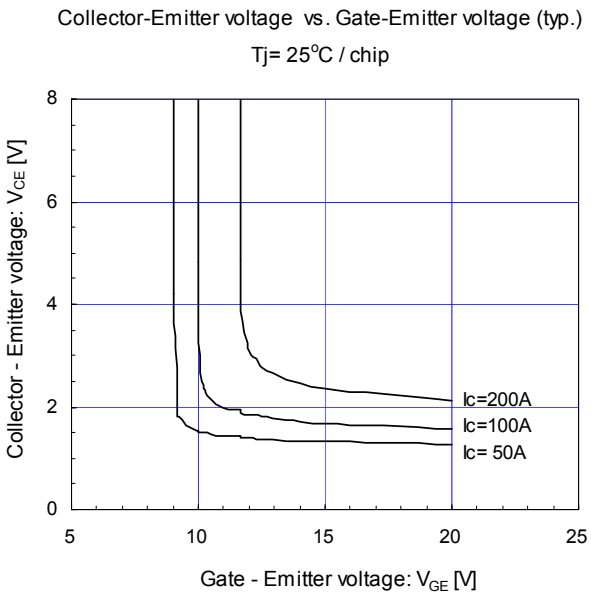


Fig. 2-3 VCE - VGE characteristics (Tj=25°C)

2.2 Switching characteristics

As the IGBT is generally used for switching, it is important to fully understand the turn-on and turn-off switching characteristics in order to determine “switching loss” (power dissipation loss at switching). It is also important to remember that these characteristics are affected by various parameters when determining operating conditions.

The circuit shown in Fig.2-4 is used to measure the four parameters of switching time, t_r, t_{on}, t_f and t_{off} as shown in Fig.2-5.

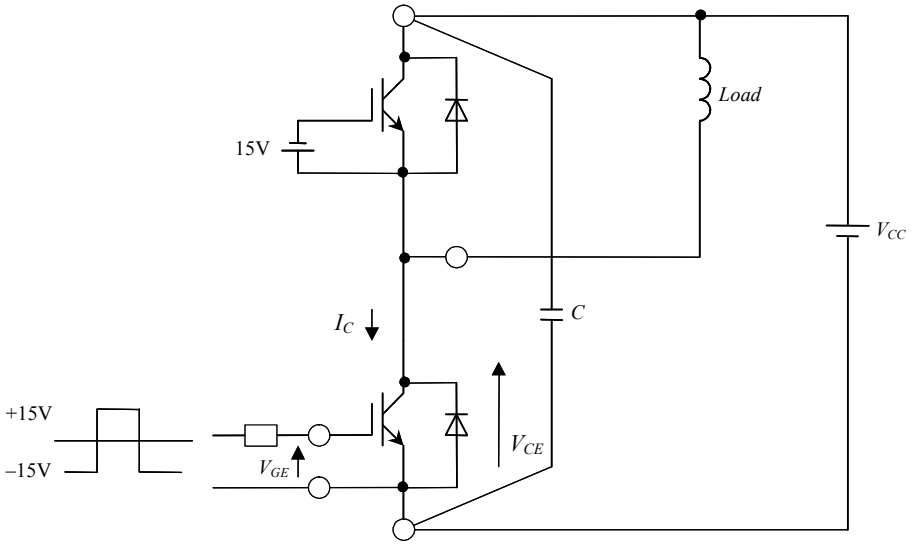


Fig. 2-4 Switching characteristics measuring circuit.

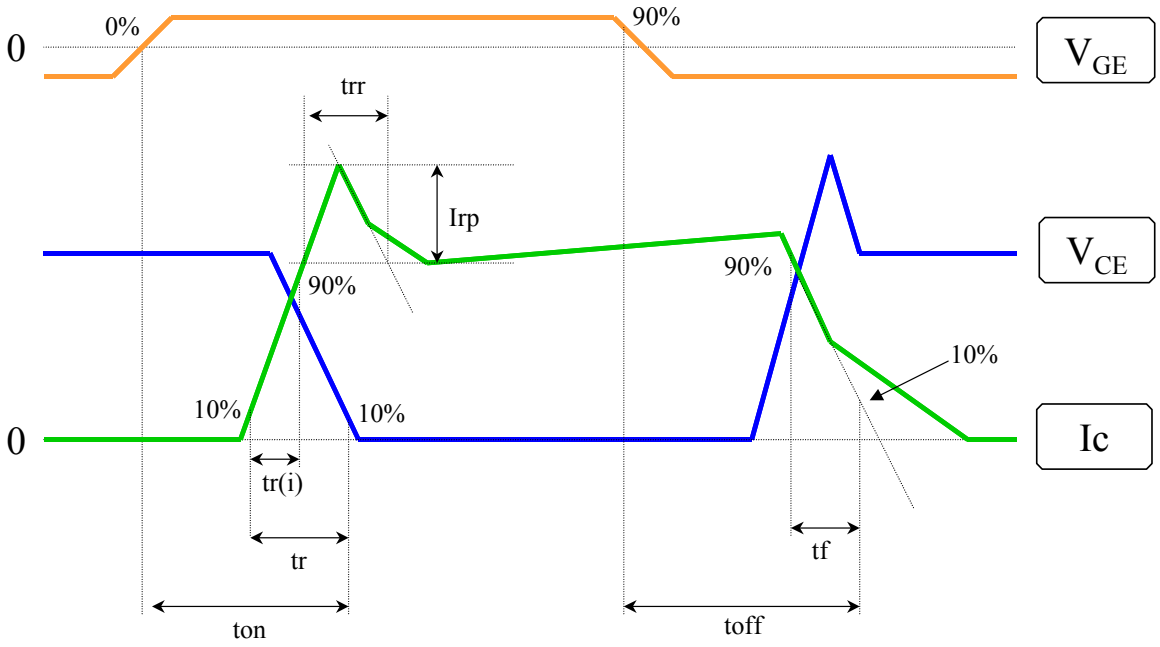


Fig. 2-5 Definition of switching time

The relationship between switching time and collector current is shown in Fig.2-6 (T_j = 125°C) and Fig. 2-7 (T_j =150°C). At greater collector currents or higher T_j, the switching time increases causing higher losses. The effect of gate resistance (R_g) vs. switching time can be seen in Fig.2-8. When the IGBT is installed in an inverter circuit or other equipment, should the switching time (especially t_{off}) become too long, it may exceed the dead time of the upper and lower transistors, thereby causing a short-circuit. It is also important to be aware that if the switching time (t_f) is too short, the transient current change rate (di/dt) will increase and then the circuit inductance may cause a high turn-off spike voltage (L di/dt). This spike voltage will be added to the applied voltage. In this case, destruction may be caused by overvoltage out of RBSOA.

Switching loss (Eon, Eoff, Err) occurs every time an IGBT is turned on or off, therefore it is important to minimize this loss as much as possible. As can be seen in Fig.2-9, the greater the collector current or the higher the T_j, the greater the switching loss will be. In the same way, switching losses depend on gate resistance R_G as shown in Fig.2-10.

Like these, IGBT characteristics are varied by collector current, T_j or R_g. Therefore, you should design your equipments in consideration with the above-mentioned characteristics.

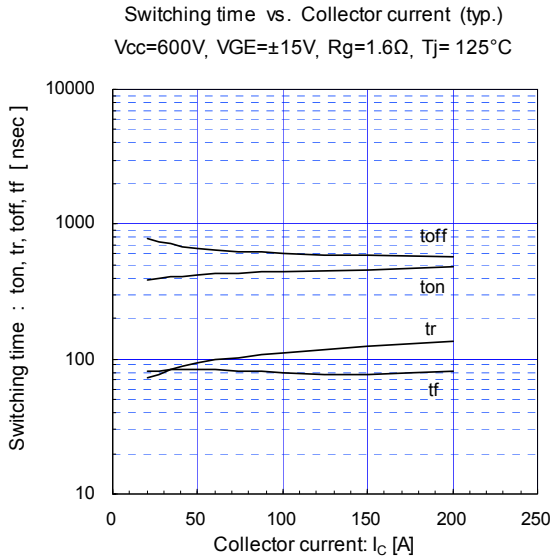


Fig. 2-6 Switching time - I_C characteristics (Tj=125°C).

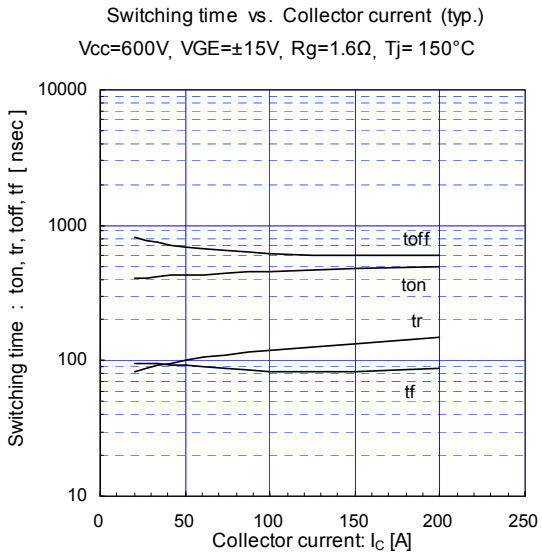


Fig. 2-7 Switching time - I_C characteristics (Tj=150°C).

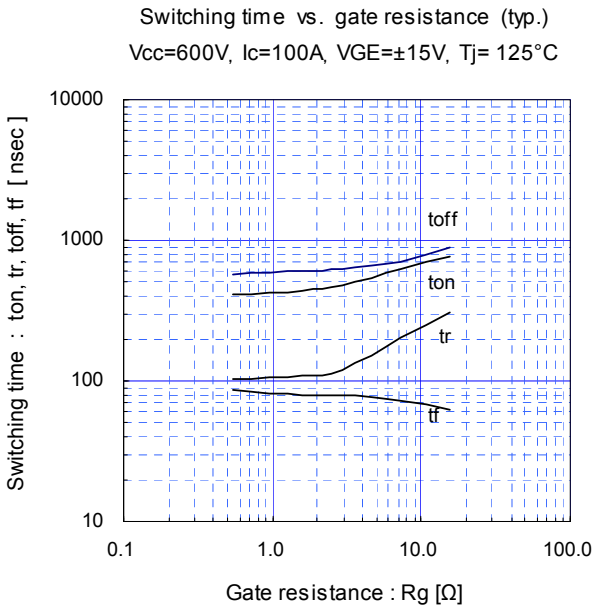


Fig. 2-8 Switching time - R_G characteristics (Tj=125°C).

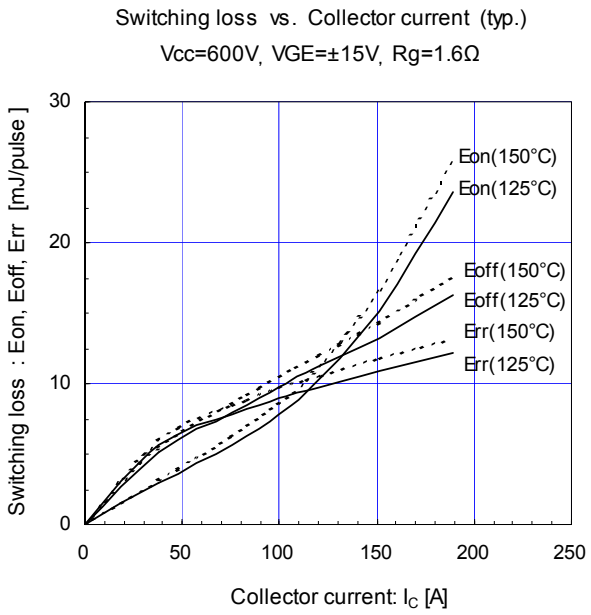


Fig. 2-9 Switching loss - I_C characteristics

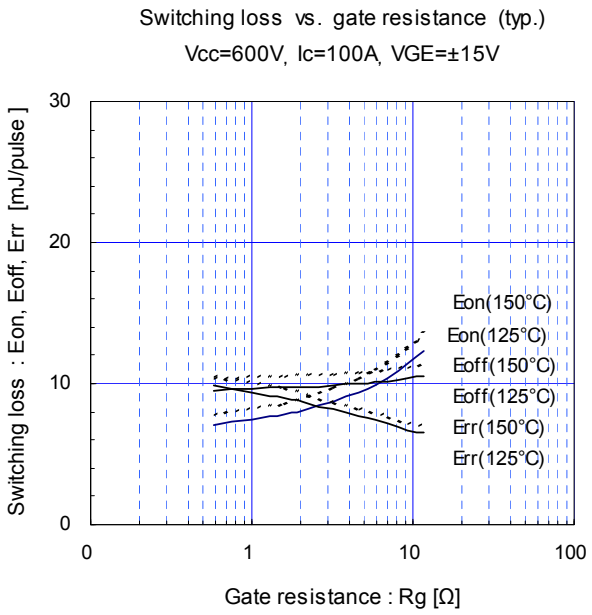


Fig. 2-10 Switching loss - R_G characteristics

2.3 Capacitance characteristics

The gate charge capacity (Q_g) characteristics, with the main circuit supply voltage (V_{CC}) as a parameter, are shown in Fig.2-11. Here can be seen how the collector-emitter voltage (V_{CE}) and gate-emitter voltage (V_{GE}) fluctuates when the gate charge charges. Since the gate charge capacity indicates the size of the charge required to drive an IGBT, it can be used to determine the power-supply capacity of the drive circuit.

Fig.2-12 shows the capacitance of each of the IGBT's junctions: gate-emitter input capacitance (C_{ies}), collector-emitter output capacitance (C_{oes}) and collector-gate reverse transfer capacitance (C_{res}).

Use these characteristics along with Q_g to design your drive circuits.

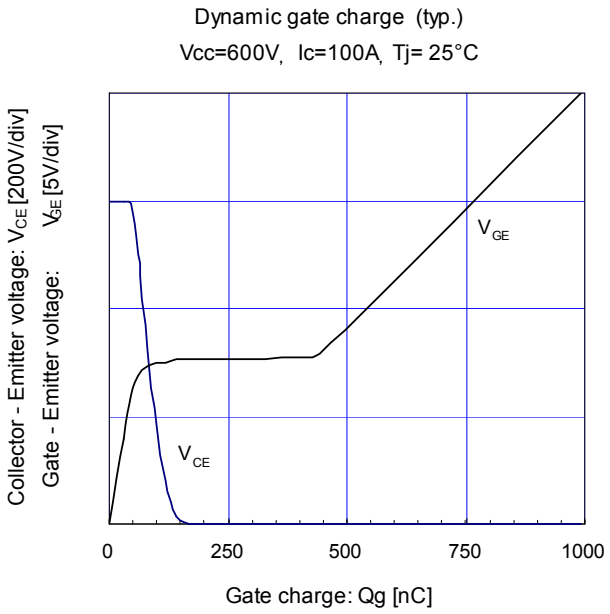


Fig.2-11 V_{CE}, V_{GE} - Q_g characteristics

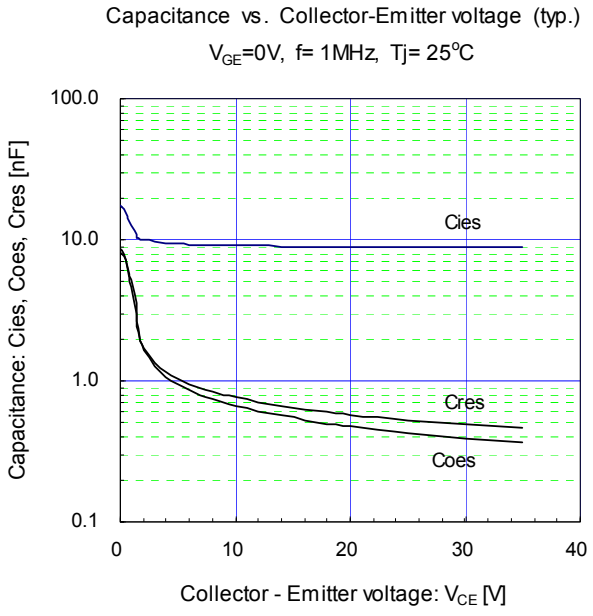


Fig.2-12 Cies, Coes, Cres - VCE characteristic

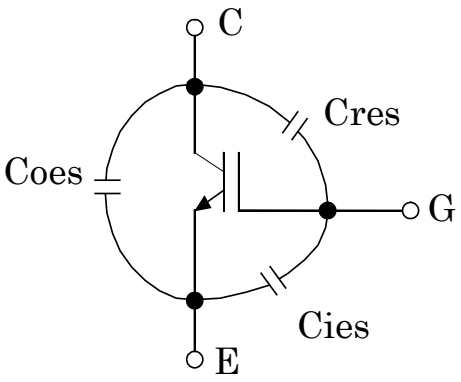


Fig.2-13 Junction capacitance.

2.4 Reverse biased safe operating areas

When turned off, the IGBT has a safe operating area defined by V_{CE} an I_c called the “reverse bias safe operating area” or RBSOA. This area is shown by the solid line in Fig.2-14.

It is important to design a snubber circuit that will keep V_{CC} and I_C within the limits of RBSOA when the IGBT is turned off.

Even in the case of a short-circuit (non-repetitive), an IGBT still has a safe operating area defined by V_{CE} an I_c called the “short circuit safe operating area” or SCSOA. SCSOA is various for each IGBT series. Refer to the technical data in details.

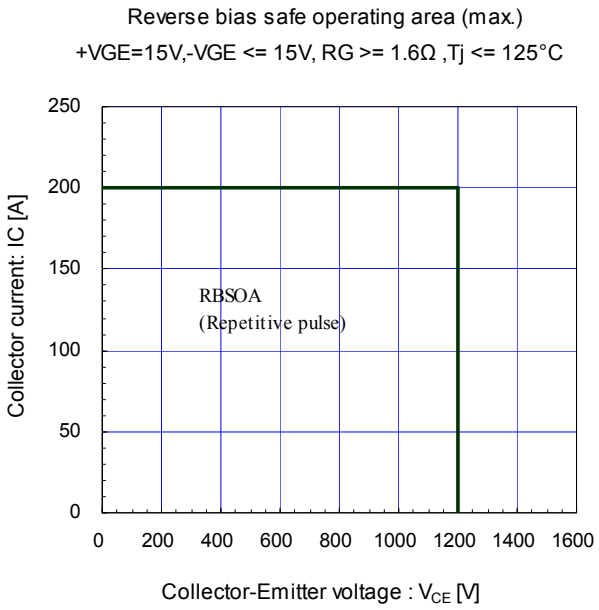


Fig. 2-14 Reverse bias safe operation area.

2.5 Internal diode (FWD) characteristics

The IGBT module has a high-speed diode (Free Wheel Diode / FWD) connected in anti-parallel with the IGBT for operating with reverse polarity. This FWD has the V_F-I_F characteristic shown in Fig.2-15, the reverse recovery characteristic (t_{rr}, I_{rr}) shown in Fig.2-16, and the switching power loss characteristic (E_{rr}) at reverse recovery shown in Fig.2-9 and Fig.2-10.

Use these characteristics to calculate the power loss in the FWD as well as the IGBT, but remember that the FWD characteristics vary in accordance with the collector current and temperature.

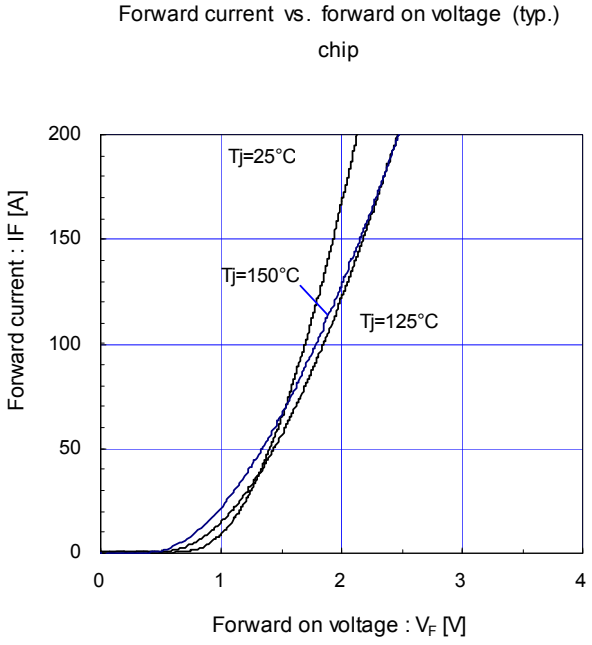


Fig. 2-15 V_F - I_F characteristics

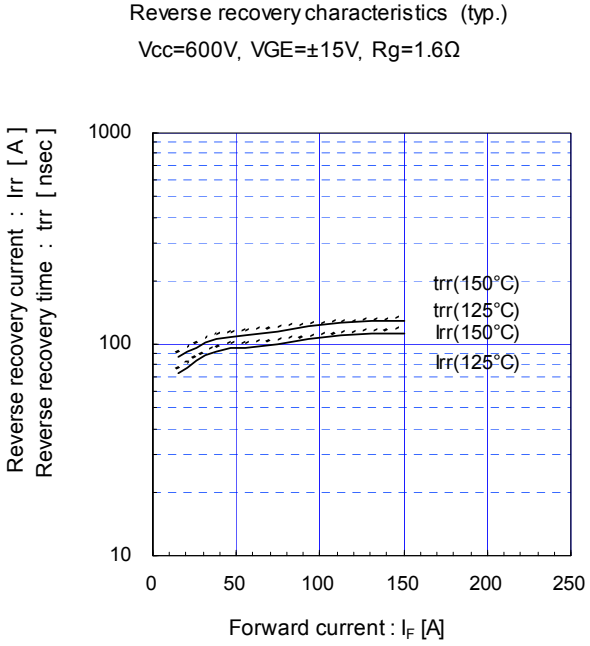


Fig. 2-16 t_{rr} , I_{rr} - I_F characteristics.

2.6 Transient thermal resistance characteristics

The transient thermal resistance characteristics, used to calculate the temperature rise of a module and to design a heat sink, are shown in Fig. 2-17.

The characteristics in the figure vary according to each individual IGBT and FWD.

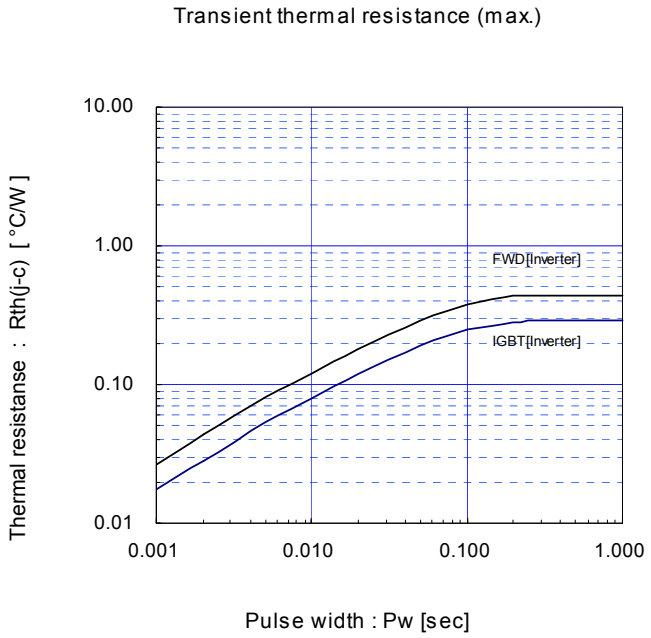


Fig. 2-17 Transient thermal resistance.

Chapter 3

IGBT Module Selection and Application

CONTENTS

This section explains relevant IGBT module selection and application.

1 Selection of IGBT module ratings

When using IGBT modules, it is important to select modules which having the voltage and current ratings most suited for the intended application.

1.1 Voltage rating

The IGBT voltage rating closely depends on the input voltage of the equipment in which it will be installed. Table 3-1 lists IGBT voltage ratings and applicable input voltages. Use this table as a reference when selecting modules for a particular voltage application.

Table 3-1 IGBT rated voltage and applicable input voltage

	Area		IGBT rated voltage V_{CES}		
			600V	1200V	1700V
Line voltage (Input voltage AC)	Asia	Japan	200V	400V, 440V	690V (Hgih voltage supply for Industry, wind-power generation etc.)
		South Korea	200V, 220V	380V	
		China	220V	380V	
	North America	U.S.A	120V, 208V, 240V	460V, 480V	
		Canada	120V, 208V, 240V	575V	
	Europe	U.K	230V	400V	
		France	230V	400V	
		Germany	230V	400V	
		Russia	220V	380V	

1.2 Current rating

When the IGBT module's collector current increases, consequently so will the $V_{CE(sat)}$ and the power dissipation losses.

Simultaneously, there will be an increase in the switching energy, resulting in an increase in the chip and module temperature.

It is necessary to control the collector current in order to keep the junction temperature below maximum junction temperature (T_{jmax}), taking into account of the heat generation of both conduction and switching energy disspipation. When designing a power conversion equipment, it should be noted the fact that as the switching frequency increases, so will the switching loss and the amount of heat generated. It is recommended to keep the collector current at or below the maximum rating for the reasons stated above. This also provides a more economical design.

2 Static electricity countermeasures

The V_{GE} of an IGBT is rated ± 20V. If an IGBT is subjected to a V_{GES} that exceeds this rated value, then there is a danger that the module might be destroyed. Therefore, ensure that the voltage between the gate and emitter is never greater than the maximum allowable value.

When an IGBT is installed and voltage is applied between the collector and emitter while the gate emitter connection is open as shown in Fig. 3-1, depending on changes in the electric potential of the collector, the current (i) will flow, causing the gate's voltage to rise turning the IGBT on.

Under these circumstance, since the voltage potential between the collector and emitter is high, the IGBT could overheat and be destroyed.

On an installed IGBT, if the gate circuit is faulty or completely inoperative (while the gate is open), the IGBT may be destroyed when a voltage is applied to the main circuit. In order to prevent this destruction, it is recommended that a 10KΩ resistor (R_{GE}) be connected between the gate and the emitter.

Furthermore, since IGBT modules have a MOS structure that is easily destroyed by static electricity, observe the following points of caution.

1) When handling IGBTs, hold them by the case and do not touch the terminals.
2) If the terminals are connected by some conductive material, do not remove the material until immediately before wiring.
3) It is recommended that any handling of IGBTs be done while standing on a grounded mat.
4) Before touching a module's terminal, discharge any static electricity from your body or clothes by grounding through a high capacity resistor (1MΩ) i.e. ESD grounding strap.
   When soldering, in order to protect the module from static electricity, ground the soldering iron through a low capacity resistor.

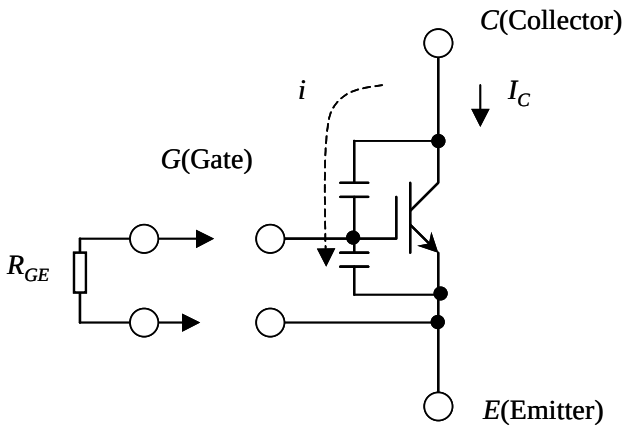


Fig. 3-1 Gate charging from electric potential of collector.

3 Designing protection circuits

Since IGBT modules may be destroyed by overcurrent, overvoltage or other abnormality, it is necessary to design protection circuits.

It is important when designing this circuits that module's characteristics are fully taken into consideration, since an inappropriate circuit will allow the module to be destroyed. For example, the overcurrent cut-off time may be too long or the capacitance of the snubber circuit's capacitor may be too small.

For more details on overcurrent and overvoltage protection methods, refer to chapter 5 of this manual.

4 Designing heat sinks

As the maximum allowable junction temperature ($T_{j(max)}$) of an IGBT modules is fixed, an appropriate heat sink must be selected to keep them at or below these values.

When designing appropriate cooling, first calculate the loss of a single IGBT module, then based on that loss, select a heat sink that will keep junction temperature (T_j) within the required limits.

If the IGBT module is not sufficiently cooled, the temperature may exceed $T_{j(max)}$ during operation and destroy the module. For more information on IGBT power loss calculation and heat sink selection methods, refer to chapter 6 of this manual.

5 Designing drive circuits

It cannot be emphasized enough, that it is the design of the drive circuit that ultimately determines the performance of an IGBT. It is important that drive circuit design is also closely linked to protection circuit design.

Drive circuits consists of a forward bias voltage section to turn the IGBT on, and a reverse bias voltage section to accelerate and maintain turn-off. Remember that the characteristics of the IGBT change in accordance with the conditions of the circuit. Also, if the circuit is wired improperly, it may cause the module to malfunction. For more information on how to design the best drive circuits, refer to Chapter 7 of this manual.

6 Parallel connection

In high capacity converters/inverters and other equipment that needs to control large currents, it may be necessary to connect IGBT modules in parallel.

When connected in parallel, it is important that the circuit design allows for an equal flow of current to each of the modules. If the current is not balanced among the IGBTs, a higher current may build up in just one device and destroy it.

The electrical characteristics of the module as well as the wiring design, change the balance of the current between parallel connected IGBTs. In order to help maintain current balance it may be necessary to match the $V_{CE(sat)}$ values of all devices.

For more detailed information on parallel connections, refer to Chapter 8 of this manual.

7 Mounting notes

When mounting IGBT modules on designated equipment, note the following:

1. When mounting an IGBT module on a heat sink, first apply a thermal grease or equivalent material to the module's base and then secure it properly to the heat sink by tightening the specified screws using the recommended torque. Use a heat sink with a mounting surface finished to a roughness of 10μm or less and a flatness of 50μm or less between screw mounting pitches. For more details, refer to Chapter 6 of this manual.
2. Avoid wiring designs that places too much mechanical stress on the module's electrical terminals.

8 Storage and transportation notes

8.1 Storage

1) The IGBT modules should be stored at an ambient temperature of 5 to 35°C and humidity of 45 – 75%. If the storage area is very dry, a humidifier may be required. In such a case, use only deionized water or boiled water, since the chlorine in tap water may corrode the module terminals.
2) Avoid exposure to corrosive gases and dust.
3) Rapid temperature changes may cause condensation on the module surface. Therefore, store modules in a place with minimal temperature changes.
4) During storage, it is important that nothing be placed on top of the modules, since this may cause excessive external force on the case.
5) Store modules with unprocessed terminals. Corrosion may form causing presoldered connections to have high contact resistance or potential solder problems in later processing.
6) Use only antistatic containers for storing IGBT modules in order to prevent ESD damage.

8.2 Transportation

1) Do not drop or jar modules which could otherwise cause mechanical stress.
2) When transporting several modules in the same box or container, provide sufficient ESD padding between IGBTs to protect the terminals and to keep the modules from shifting.

9 Reliability notes

Generally, when the power converters such as inverters are in operation, the temperature rises and falls repeatedly in the IGBT module installed in the system. Accordingly, the IGBT module is exposed to the thermal stress caused by thistemperature swing and so its life span depends on the operating conditions. Therefore, the expected thermal cycling lifetime of IGBT module must be designed to be longer than system lifetime design.

In general, the temperature swing of the IGBT module has to be checked and the expected IGBT module lifetime should be predicted based on the power cycle capability. If the life design is not well investigated, the life span of the IGBT module may result shorter than expectation which may cause long-term reliability issue of system. Therefore, it is strongly recommended to investigate the the IGBT module temperature cycling design to matchthe required reliability criteria.

For more detailed information on reliability notes, refer to Chapter 11 of this manual.

10 Additional notes

1) The gate drive voltage (V_{GE}) should be measured at the terminals of the module to verify that a predetermined voltage is being applied. (Measurement at the output stage of the drive circuit may lead to a voltage that is unaffected by the voltage drops across the transistors and other components used at the output stage of the drive circuit. Consequently, if the predetermined voltage (V_{GE}) is not being applied to the IGBT gate, this lower (V_{GE}) voltage could pass unnoticed, leading to device destruction.

2) Measure the surge and other voltages appearing during turn-on and turn-off at the module terminals. If measured terminals are defined on the specification, measure the voltages at defined terminals.

3) Use the product within the tolerances of the absolute maximum ratings (voltage, current, temperature etc). Particularly, if a voltage higher than V_{CES} is applied to the module, an avalanche breakdown could occur, resulting in device destruction.

4) As a precaution against the possible accidental destruction of the device, insert a fuse or breaker of the appropriate rating between the commercial power source and the semiconductor device.

5) Before using the IGBT, acquire a full understanding of its operating environment to verify that its matched long term reliability requirement. If the product is used exceeding its product lifetime, the device could be destroyed before the intended useful life of the equipment expires.

6) Use this IGBT within its power-cycle life capability. Power cycle capability is classified to delta-Tj mode, which is stated as above, and delta-Tc mode. Delta-Tc mode is due to rise and down of case temperature (Tc), and depends on cooling design of equipment, which use this product. In application, which has such frequent rise and down of Tc, well consideration of product lifetime is necessary.

7) Avoid using the product in locations where corrosive gases are present. The warranty covering the functionality, appearance and other aspects of the product will be voided if it is used in environments where acids, organic substances or corrosive gases (such as hydrogen sulfide and sulfur dioxide) are present.

8) Do not allow the primary and control terminals of the product IGBT to be deformed by stress. A deformed terminal could cause a defective contact or other fault.

9) Select the correct terminal screws for the module according to the outline drawing. Using longer screws could damage the device.

10) If only a FWD is used and an IGBT is not used (as in a chopper circuit application), apply a reverse bias voltage of -5V or higher (-15V recommended, -20V maximum) between G and E of the IGBT out of service. An insufficient reverse bias voltage could cause the IGBT to false triggered due to dV/dt during reverse recovery of the FWD, resulting in device destruction.

11) A high turn-on voltage (dv/dt) could cause the IGBT in the opposing arm to turn on falsely. Use the product under optimal gate drive conditions (such as $+V_{GE}$, $-V_{GE}$, and R_G, $C_{GE)}$ to prevent false turn-on.

12) Do not apply excessive stress to the primary and control terminals of the product when installing it in equipment. The terminal structure could be damaged.

13) Use this product with keeping the cooling fin's flatness between screw holes within 50μm at 100mm and the roughness within 10μm. Also keep the tightening torque within the limits of this specification. Too large convex of cooling fin may cause isolation breakdown and this may lead to a critical accident. On the other hand, too large concave of cooling fin makes gap between this product and the fin bigger, then, thermal conductivity will be worse and over heat destruction may occur.

14) If excessive static electricity is applied to the control terminals, the devices may be broken. Implement some countermeasures against static electricity.

15) In case of mounting this product on cooling fin, use thermal grease or equivalent cooling methods to secure thermal conductivity. If the thermal grease amount was not enough or greasing method was not suitable, its spreading will not be enough, then, thermal contact resistance between IGBT module base and heatsink may have an issue which results thermal run away destruction in worst case. Experimental confirmation of grease spreading state at the thermal contact is recommended before applying to the actual product. (Spreading state of the thermal compound can be confirmed by removing this product after mounting.)

16) The gate resistance R_G described in the specification sheet is one of example values to achieve the highest performance of minimized switching energy. In practical application, the optimum R_G depends on the circuit setup and/or system environment. Therefore, the gate resistance R_G should be selected with consideration of switching losses, EMC/EMI, spike voltage, spike current and unexpected oscillation and so on based on system requirement and IGBT module specification.

17) More references of notes. cautions and warnings in detail can be found in each specification provided for specific products. Following these contents is also recommended to take into account of system design because information in this section describes a part of important notifications.

Chapter 4

Troubleshooting

CONTENTS

This section explains IGBT troubleshooting and failure analysis.

1 Troubleshooting

Incorrect wiring or mounting of an IGBT in an inverter circuit could cause module destruction. Because a module could be destroyed in many different ways, once the failure has occurred, it is important to first determine the cause of the problem, and then to take the necessary corrective action. Table 4-1, illustrates how to determine a module's failure modes as well as the original causes of the trouble by observing irregularities outside of the device. First of all, compare the device estimated failure mode to the table when an IGBT is destroyed. Fig.4-1(a-f) was prepared as a detailed guide (analysis chart), and should be used to help investigate the destruction when you cannot determine the cause by using Table 4-1. Typical failure modes and troubleshooting are described in section 4-3 and can be used to assist in finding the cause.

Table 4-1 Causes of device failure modes

External abnormalities		Cause		Device failure mode	Further checkpoints
Short circuit	Arm short circuit	Short circuit destruction of one element		Outside SCSOA	Confirm waveform (locus) and device ruggedness match during an arm short circuit.
	Series arm short circuit	Gate or logic Circuit malfunction	Noise, etc.	Outside SCSOA	Check for circuit malfunction. Apply the above.
		dv/dt	Insufficient gate reverse bias. Gate wiring too long	Overheating	Check for accidental turn-on caused by dv/dt.
		Dead time too short	Insufficient gate reverse bias. Date time setting error	Overheating	Check that elements t_{off} and dead time match.
	Output short circuit	Miss wiring, abnormal wire contact, or load short circuit.		Outside SCSOA	Check conditions at time of failure. Check that device ruggedness and protection circuit match. Check wiring condition.
	Ground short	Miss wiring, abnormal wire contact		Outside SCSOA	
Overload		Logic circuit malfunction Overcurrent protection circuit setting error		Overheating	Check logic circuit. Check that overload current and gate voltage match. If necessary, adjust overcurrent protection level.
Over Voltage	Excessive input voltage	Excessive input voltage Insufficient overvoltage protection		C-E Overvoltage	If necessary, adjust overvoltage protection level.
	Excessive spike voltage	Switching turn-off		Outside RBSOA	Check that turn-off operation (loci) and RBSOA match. If necessary, adjust overcurrent protection level.
		FWD commutation	High di/dt resulting	C-E Overvoltage	Check that spike voltage and device ruggedness match. If necessary, adjust snubber circuit.
			Transient on state (Short off pulse reverse recovery)		Check logic circuit. Gate signal interruptions resulting from noise interference.
Drive supply voltage drop		DC-Dc converter malfunction		Overheating	Check circuit.
		Drive voltage rise is too slow.		Overheating	
		Disconnected wire		Overheating	

External abnormalities		Cause		Device failure mode	Further checkpoints
Gate overvoltage		Static electricity Spike voltage due to excessive length of gate wiring		Avalanche Overvoltage	Check operating conditions (anti-static protection). Check gate voltage.
Overheating	Overheating	Loose terminal screw or cooling fan shut down		Overheating	Check cooling conditions. Check logic circuit. Logic circuit malfunction
	Thermal runaway	Logic circuit malfunction		Overheating	
Stress	Stress	The soldering part of the terminal is disconnected by the stress fatigue.	Stress from external wiring	Disconnection of circuit	Check the stress and mounting parts.
	Vibration		Vibration of mounting parts		
Reliability (Life time)		The application condition exceeds the reliability of the module.		Destruction is different in each case.	Refer to Fig.4-1 (a-f).

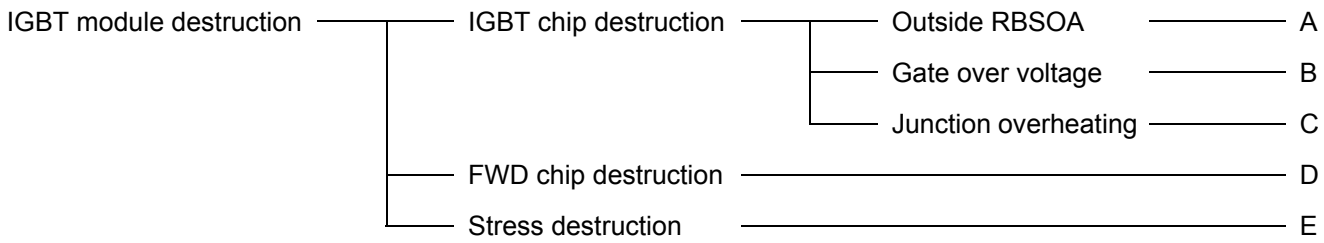


Fig.4-1 (a) IGBT module failure analysis

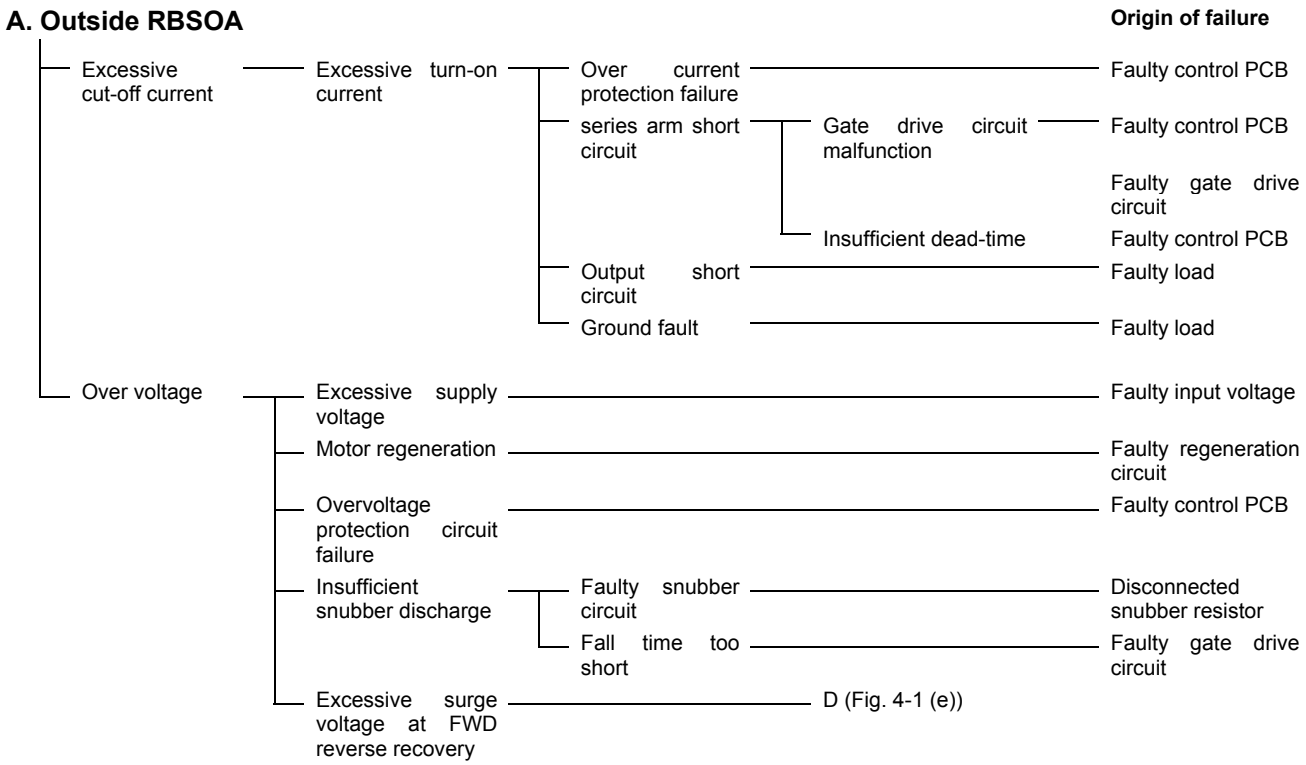


Fig.4-1 (b) Mode A: Outside RBSOA

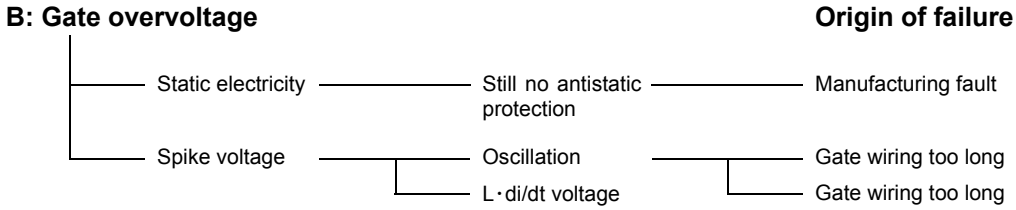


Fig.4-1 (c) Mode B: Gate overvoltage

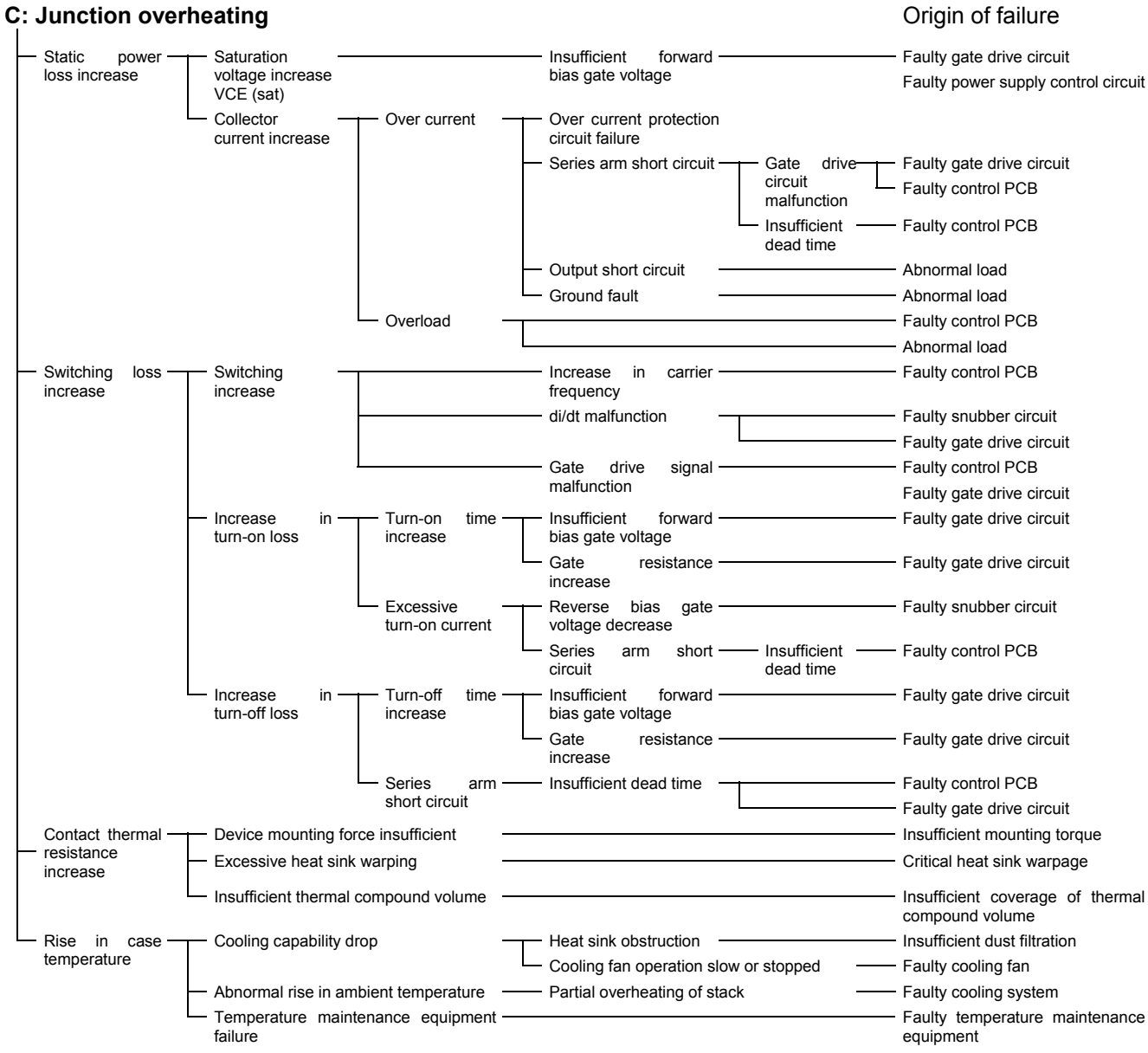


Fig.4-1 (d) Mode C: Junction overheating

D: FWD destruction

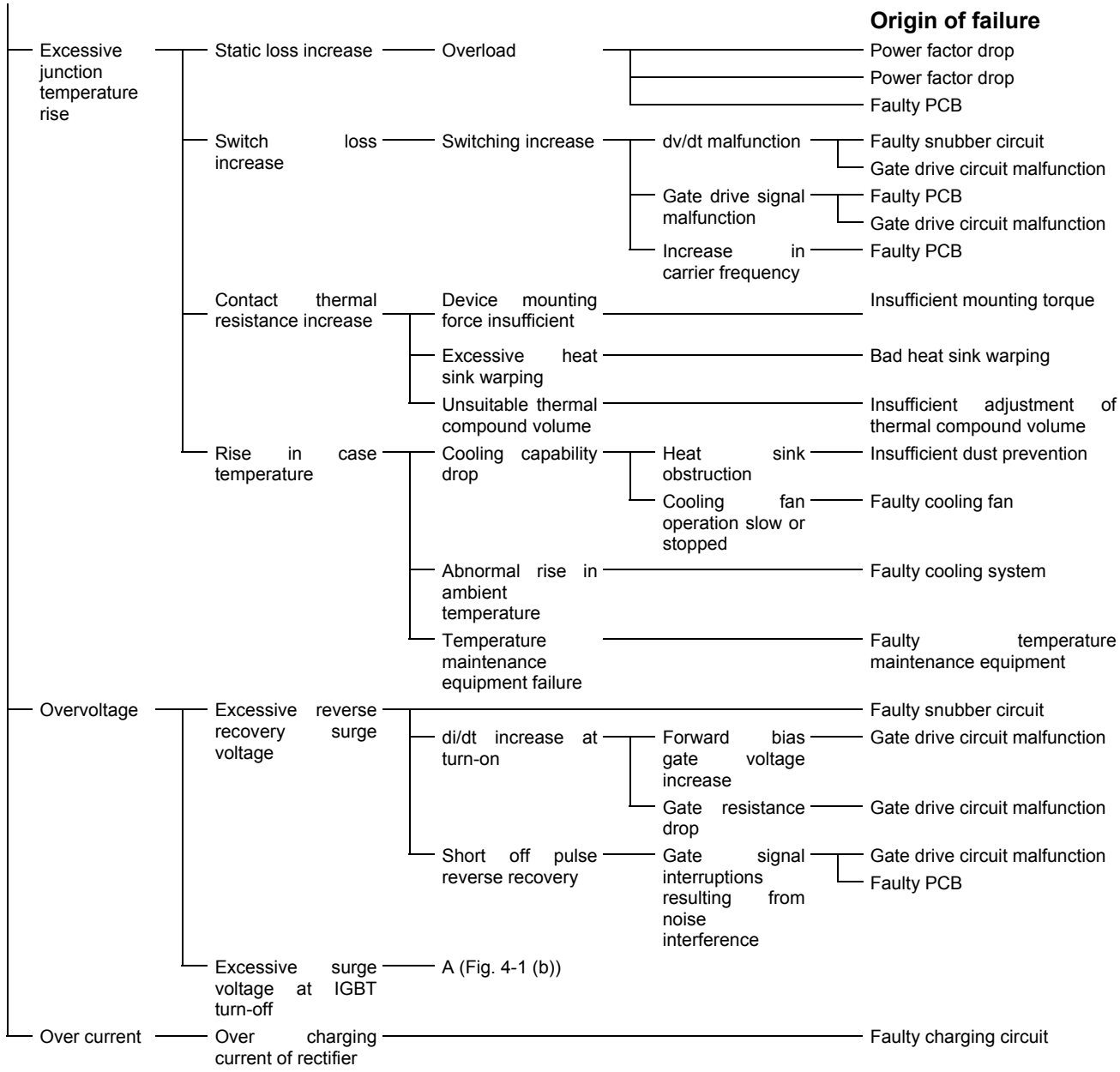


Fig.4-1 (e) Mode D: FWD destruction

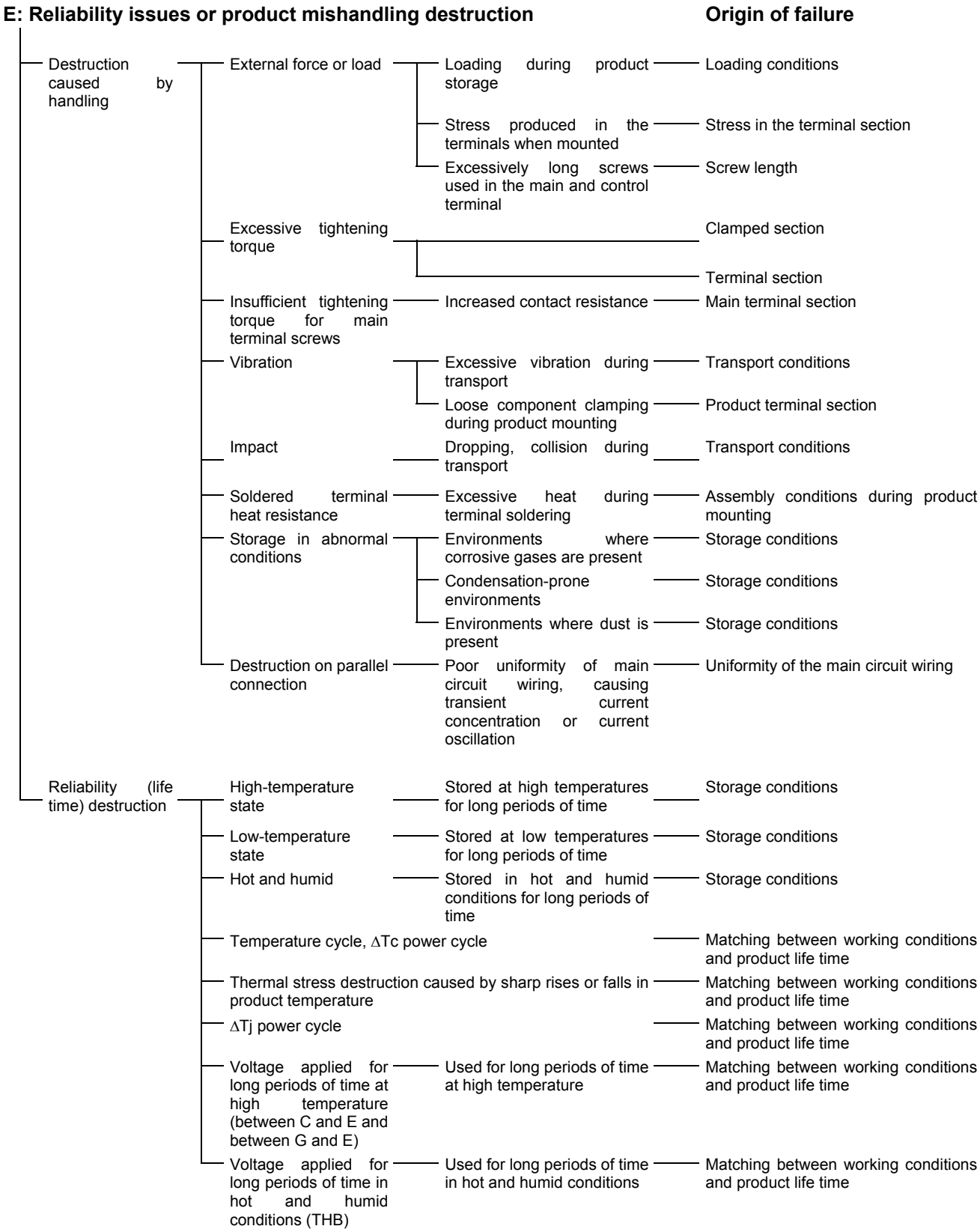


Fig.4-1 (f) Mode E: Reliability issues or mishandling destruction

2 IGBT test procedures

An IGBT module that has been found to be faulty can be checked by testing it on a transistor characteristics measuring device called a "transistor curve tracer (CT)."

(1) Leakage current between gate and emitter, and threshold voltage between gate and emitter
(2) Short circuit, breakdown voltage, open circuit between collector and emitter (Short gate and emitter.)

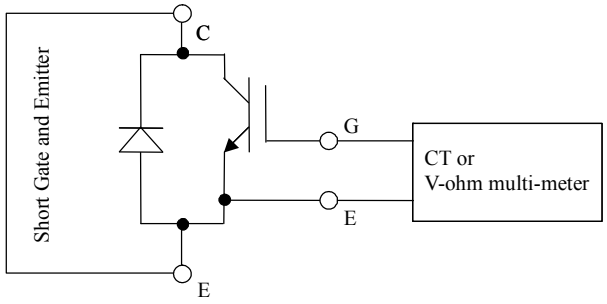


Fig. 4-1 G-E (gate) check

If a CT is not available, other test equipment, such as a Volt-ohm multi-meter that is capable of measuring voltage/resistance and so forth to determine a failure, can be used to help diagnose the destruction.

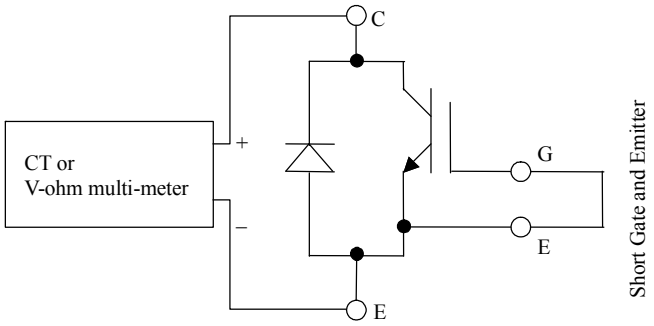


Fig. 4-2 C-E check

2.1 G-E check

As shown in Fig.4-2, measure the leakage current or resistance between G and E, with C and E shorted to each other. (Do not apply a voltage in excess of 20V between G and E). If the V-ohm multi-meter is used, verify that the internal battery voltage is not higher than 20V.)

If the product is normal, the leakage current reading should be on the order of several hundred nano-Amps. (If the V-ohm multi-meter is used, the resistance reading would range from several tens MΩ to infinite. In other situations, the device has most likely broken down. (Generally, device destruction is represented by a short between G and E.)

2.2 C-E check

As shown in Fig.4-3, measure the leakage current or resistance between C and E, with a short between G and E. Be sure to connect the collector to (+) and the emitter to (-). Reverse connections will energize the FWD, causing C and E to be shorted to each other.

If the module is normal, the leakage current reading should read below the I_{CES} maximum specified in the datasheet. (If the V-ohm multi-meter is used, the resistance reading would range from several ten MΩ to infinity. In other situations, the device has most likely broken down. (Generally, device destruction is represented by a short between C and E.)

Note:

Never perform withstand voltage measurement between the collector and gate. It might cause the dielectric destruction of the oxide layer by applying excess voltage.

3 Typical trouble and troubleshooting

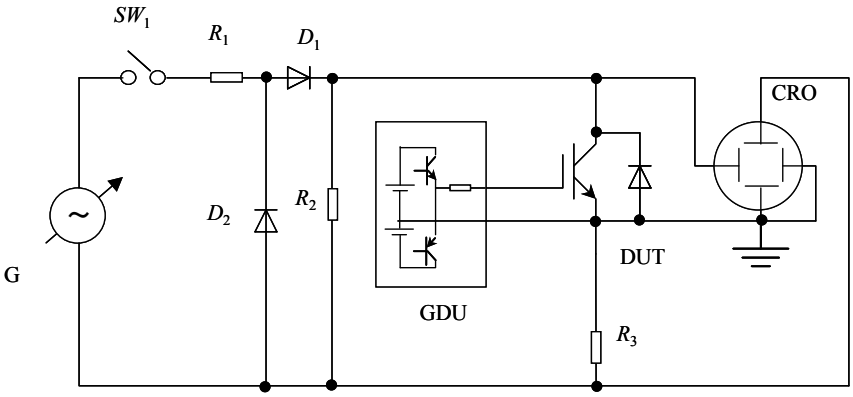
3.1 Energizing a main circuit voltage when the circuit between G and E is open

If a voltage is applied to the main circuit with the circuit between the gate and emitter open, the IGBT would be turned on autonomously, triggering large current flow to cause device destruction. Be sure to drive the device with a signal placed between G and E. This phenomenon occurs when the gate-emitter capacitance is charged through feedback capacitance Cres of the IGBT at the application of a main voltage with the circuit between G and E open, causing the IGBT to be turned on.

If the signal line is switched using a mechanical switch, such as a rotary switch, during product acceptance testing or on similar occasions, the circuit may open instantaneously between G and E at the time of switching could cause device destruction (the phenomenon described above).

When the mechanical switch chatters, a similar period is generated, leading to device destruction. To guard against such risks, be sure to discharge the main circuit voltage (between C and E) to 0V before switching the gate signal. When performing characteristics testing, such as acceptance testing, on a product comprising multiple devices (two or more), keep the gate and emitter shorted to each other on the devices other than the one under test.

Fig.4-4 shows an example of an on-voltage measurement circuit. The measurement sequence is described with reference to this measurement circuit. First, turn off the gate drive unit (GDU) (V_{GE} = 0V) and then turn on SW_1 to apply a voltage between C and E. Next, apply a predefined forward bias voltage between G and E from the GDU to energize the IGBT for measuring the on voltage. Lastly, turn off the gate circuit and then SW_1. Such sequencing will allow for safe measurement of device characteristics without risking destruction.



DUT: IGBT under test, GDU: Gate drive unit, G: Variable AC power supply
CRO: Oscilloscope, R_1, R_2: Protective resistance, R_3: Current measurement non-inductive resister
D_1, D_2: Diode, SW_1: Switch

Fig. 4-4 On voltage measurement circuit

3.2 Destruction caused by mechanical stress

If the terminals or pins are subjected to stress from a large external force or vibration, the internal electrical wiring of the product could be destroyed. Be careful by not mounting the device in an application that might be strenuous, minimize the chances of such destruction by reducing stress.

Fig.4-5 shows an example of mounting a gate drive printed circuit board (PCB) on top of the IGBT module.

As shown in (1), if the gate drive printed circuit board is mounted without clamping the PCB, the any PCB vibration could cause flexing possibly, stressing the module pins causing pin damage or internal electrical wiring damage. As shown in (2), the PCB needs to be clamped to prevent this problem. When taking this corrective action, use a dedicated fixing material having sufficient strength.

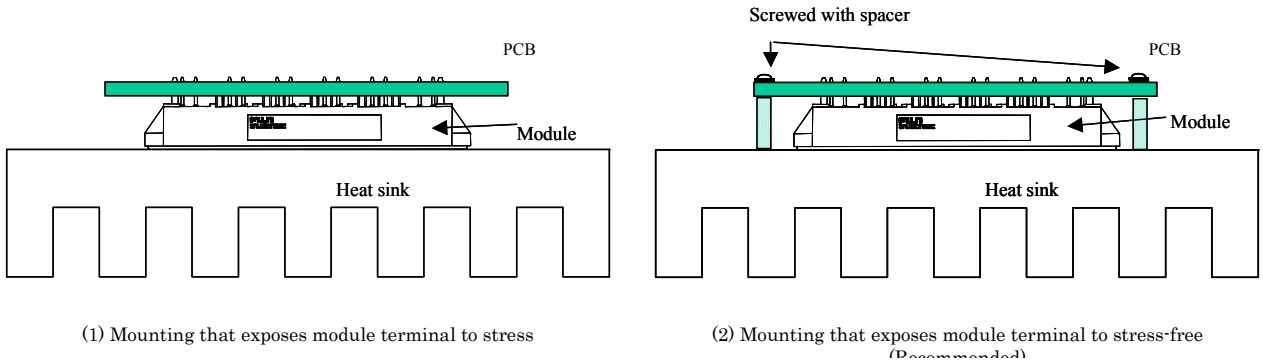


Fig. 4-5 Clamping a PCB

Fig.4-6 shows an example of main circuit wiring using a laminated bus bar. If there is a step difference between the (+) and (-) electrical wiring conductors as shown in (1), the terminals are continually exposed to upward tensile stress, causing a disconnect of the internal electrical wiring. To prevent this problem, it is necessary to insert a conductive spacer to eliminate the step difference between the conductors on the parallel plate. Furthermore, a gap in the wiring height location could also generate large tensile stress or external force to the terminals in the PCB structure. From this point, laminated bus bar or PCB needs to be mounted without tensile stress.

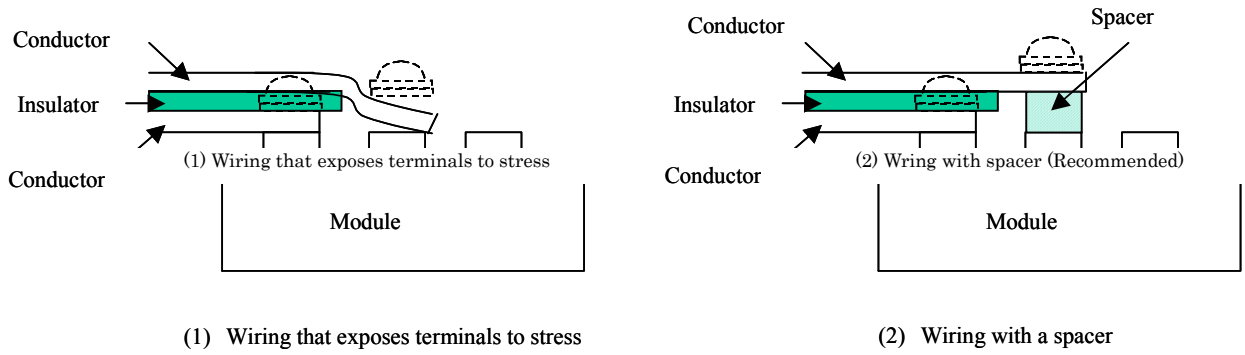


Fig. 4-6 Mounting in laminated bus bar is used

3.3 Accidental turn-on of the IGBT caused by insufficient reverse bias gate voltage $-V_{GE}$

Insufficient reverse bias gate voltage $-V_{GE}$ could cause both IGBTs in the upper and lower arms to be turned on after accidental turn-on, resulting in a short-circuit current flowing between them. A surge voltage or loss arising when this current is turned off may result in product destruction. In designing a circuit, make sure that no short-circuit currents are generated as a result of a short circuit between the upper and lower arms (recommended $-V_{GE}$ = 15V).

The occurrence of this phenomenon is described below with reference to Figs. 4-7 and 4-8.

An IGBT with $-V_{GE}$ applied is shown in Fig. 4-7. Assume that an IGBT is connected in series on the opposing arm as well, though it is not depicted. When the IGBT on the opposing arm is turned on, the FWD shown in Fig.4-7 recovers in reverse direction. Fig.4-8 shows the schematic waveform of V_{CE}, I_{CG} and V_{GE} at reverse recovery. As shown in Fig.4-8, when voltage sustained by FWD is lowered at reverse recovery, dv/dt is generated by raising the voltage between C and E at this time. This dv/dt causes current i_{CG} to flow through feedback resistance Cres between C and G and through gate resistance R_G as shown in Fig.4-7. This i_{CG} induces a potential difference of $\Delta V = R_G \times i_{CG}$ across the R_G, pushing up the V_{GE} towards the + side

as shown in Fig.4-8. If the peak voltage of V_{GE} exceeds $V_{GE\ (th)}$, the IGBT is turned on, introducing short-circuit current flow through the upper and lower arms. Conversely, no short-circuit current will flow through the upper and lower arms unless the peak voltage of V_{GE} exceeds $V_{GE\ (th)}$. This problem can be suppressed by applying a sufficient reverse bias voltage ($-V_{GE}$). Because the required value of V_{GE} depends on the drive circuit used, gate wiring, R_G and the like, check for the presence or absence of a short-circuit current flow through the upper and lower arms when designing a circuit.

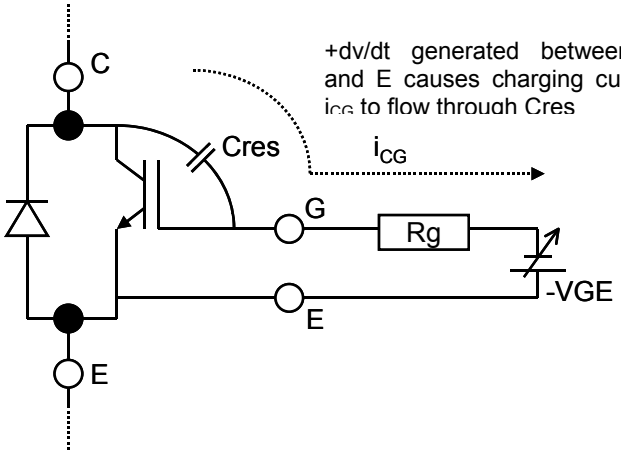


Fig. 4-7 Principles of dv/dt malfunctioning

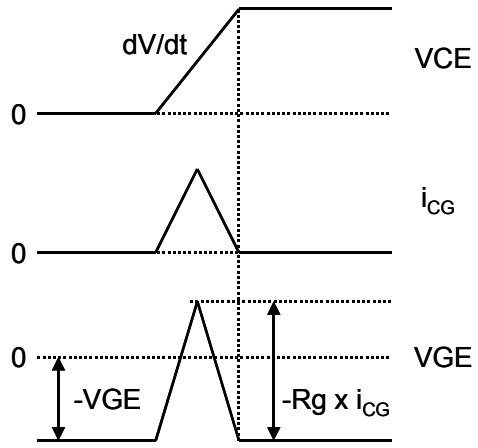


Fig.4-8 Waveforms during reverse recovery

Fig 4-9 shows an example of the method of checking for the presence or absence of the short-circuit current flow through the upper and lower arms. First, open the inverter output terminals (U, V, W) (that is, leave them under no load) as shown. Next, activate the inverter to drive the individual IGBTs. The presence or absence of the short-circuit current flow through the upper and lower arms can be determined by detecting current flow from the power line as shown. If a sufficient reverse bias current is applied, a very weak pulse current (about 5% of the rated current) that charges the device junction capacitance will be detected. With insufficient reverse bias voltage $-V_{GE,}$ this current increases.

To ensure correct determination, we recommend first detecting this current with the applied voltage $-V_{GE}$ = -15V. This eliminates the risk of false firings. Then measure the same current with the predefined value of $-V_{GE}$. If the two measurements of the current are equal, no false turn-on has occurred. In case that false turn-on is observed, a recommended solution is to increase the reverse bias voltage $-V_{GE}$ until the short-circuit current is eliminated or inserting a capacitance (C_{GE}) about half the Cies value between G and E near the module terminals. Verify the applicability of the method of the C_{GE} insertion beforehand, because it will significantly affect the switching time and switching losses. If you would like to have the similar switching losses and switching time before C_{GE} insertion, selection of approximately half R_G before C_{GE} insertion would be recommended. In this condition, no issue must be fully confirmed.

The short-circuit current flow through the upper and lower arms is caused by insufficient dead time, as well as accidental turn-on during dv/dt described above. A short-circuit current can be observed by running the test shown in Fig.4-9 while this phenomenon is present. If increasing the reverse bias voltage-V_{GE} does not help reduce the short-circuit current, take relevant action, such as increasing the dead time. (More detailed instructions can be found in Chapter 7.)

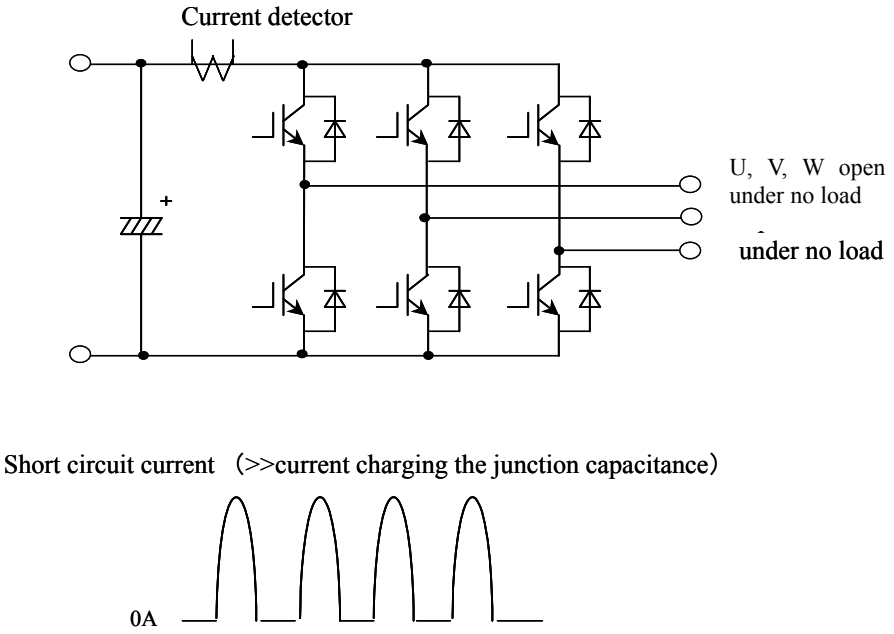


Fig. 4-9 Short-circuit current measuring circuit

3.4 Diode reverse recovery from a transient on state (Short off pulse reverse recovery)

The IGBT module contains a FWD. Paying full attention to the behavior of the FWD is very important for designing a dependable circuit. This section focuses on the less known phenomenon of short off pulse reverse recovery that could lead to product destruction.

Fig. 4-10 shows a timing chart in which an excessive surge voltage arises from short off pulse reverse recovery. According to this phenomenon, an extremely excessive reverse recovery surge voltage arises between C and E of the FWD on the opposing arm when very short off pulses (Tw) like those shown are generated after gate signal interruptions resulting from noise interferences during IGBT switching.

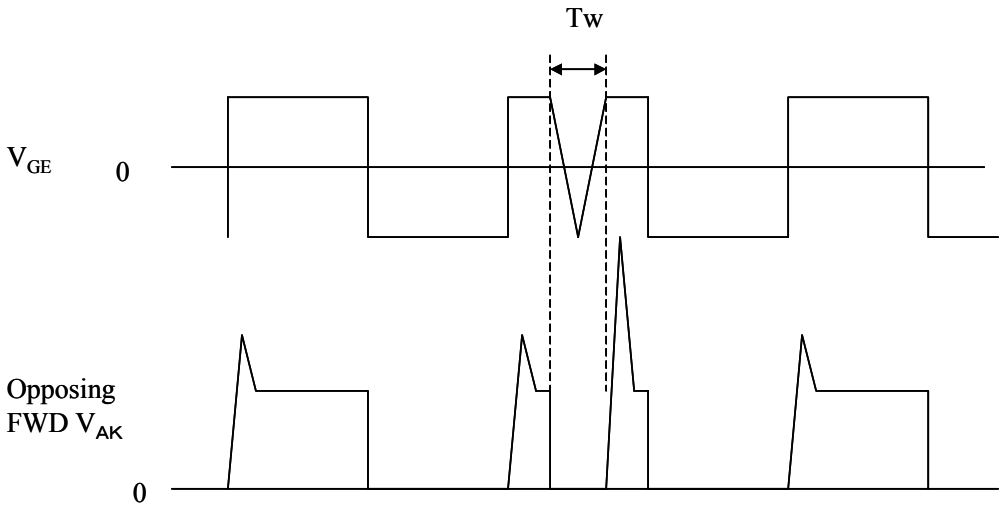


Fig. 4-10 Waveforms at short off pulse reverse recovery

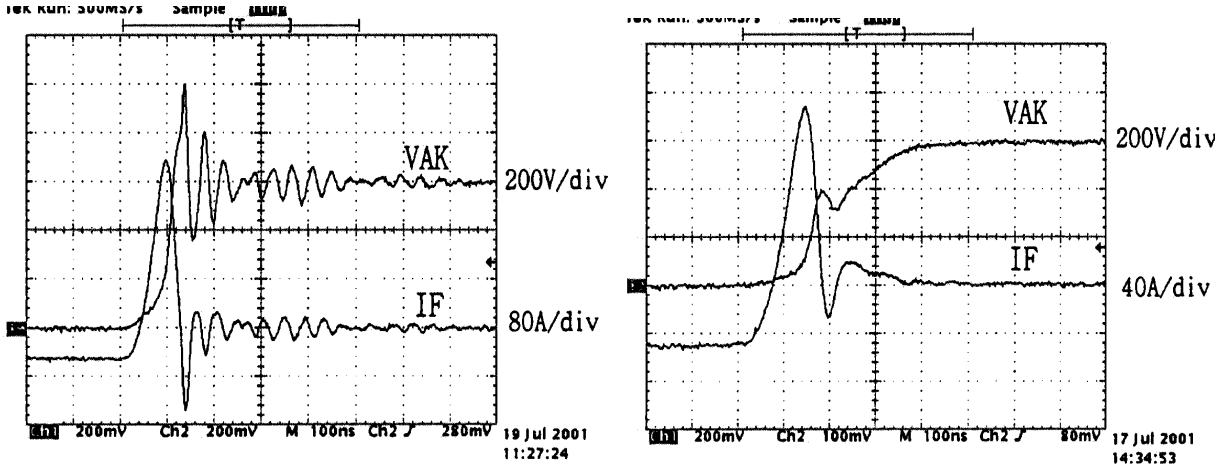
A surge voltage exceeding the guaranteed rated withstand voltage level of the module is most likely to lead to device destruction. Testing has confirmed a sharp increase in surge voltage when Tw < 1μs. Be sure not to design a circuit that will generate such short gate signal off pulses.

This phenomenon occurs because the FWD enters a state of reverse recovery very shortly after it is turned on, so that voltage application begins without a sufficient quantity of carrier stored in the FWD, with the depletion layer spreading rapidly to generate steep di/dt and dv/dt. With devices supporting an operation mode in which Tw is 1μs or shorter, verify that the surge voltage in the minimum period of Tw does not exceed the device withstand voltage.

If the surge voltage exceeds the device withstand voltage rating, take action to reduce surge voltages as follows.

- Increasing the R_G
- Cutting the circuit inductance
- Building up the snubber circuit
- Installing a C_{GE}
- Adding the clamping circuit

Fig. 4-11 shows the diode reverse-recovery waveforms when a short off pulse of 6MBI450U-120 (1200V, 450A). As shown below, surge voltage can be decreased by enlarging R_G from 1.0Ω to 5.6Ω



(1) Ron=1.0Ω (2) Ron=5.6Ω

Ed=600V, IF=50A, Tj=125°C, Tw=1μs

6MBI450U-120

Fig. 4-11 Waveforms of reverse recovery at short off pulse

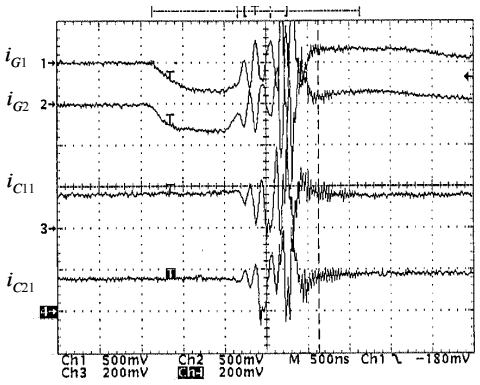
3.5 Oscillation from IGBTs connected in parallel

When products are connected in parallel, the uniformity of the main circuit wiring is very important. Without balanced wiring, concentrated transient currents could occur on the device having a shorter wiring path during switching, which could cause device destruction or degrade long-term reliability. In a main wiring circuit in which the wiring is not uniform or balanced the overall main circuit inductance will also be out of balance among the devices.

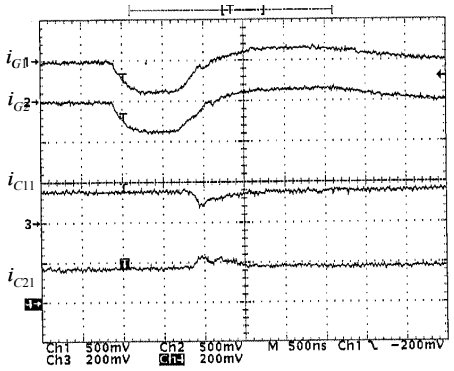
Consequently, voltages of varied potentials are generated in the individual wiring inductances from di/dt during switching, producing an abnormal oscillating current, such as a loop current, leading to possible device destruction.

Fig.4-12 (1) shows the oscillation phenomenon when the wiring inductance of the emitter portion is made extremely unbalanced. An IGBT can generate this oscillation current at the wiring loop in the emitter portion connected in parallel, this influences the gate voltage and the oscillation phenomenon which is generated by the high speed switching. A ferrite core (common mode) can be inserted in each gate emitter wiring circuit to reduce or eliminate the loop current in the emitter portion. Fig.4-12 (2) shows the waveforms with the common mode core. Note the elimination of the previous oscillation.

Give full consideration to maintaining circuit uniformity when designing main circuit wiring.



(1) When emitter inductance is unbalanced



(2) When the common mode core is inserted in gate emitter wiring

i_{G1}, i_{G2}:5A/div, i_{C11}, i_{C21}:100A/div, t:0.5μs/div, Ed=600V 1200V, 300A IGBT 2 parallel connection

Fig. 4-12 Waveforms of 2 parallel connection

3.6 Notes on the soldering process

Problems, such as melting case resin material, could result if excessive soldering temperature is applied when soldering a gate driver circuit or control circuit to the terminals of the IGBT module. Stay within normal soldering processes, avoid high exposure that exceeds maximum recommended terminal soldering defined in the specifications. (Terminal heat resistance test conditions that are covered in the general product specifications documents are listed below for reference.)

Solder temperature: 260±5°C
Dwell time: 10±1s
Cycles: 1

3.7 IGBT Module converter application

Diodes used in the IGBT modules have an I^2t rating. I^2t is a scale of the forward, non-repetitive overcurrent capability of current pulses having a very short duration (less than 10ms). Current (I) denotes the effective current, and time (t) indicates the pulse duration. If the IGBT module is used in a rectifier circuit (or converter circuit), do not exceed the maximum I^2t limits. If you approach the I^2t limits, insert a starter circuit having a resistance and a contactor connected in parallel, for example, between the AC power supply and the IGBT module. If fuse protection is used, select a fuse not exceeding rated I^2t.

3.8 Countermeasure of EMC noise

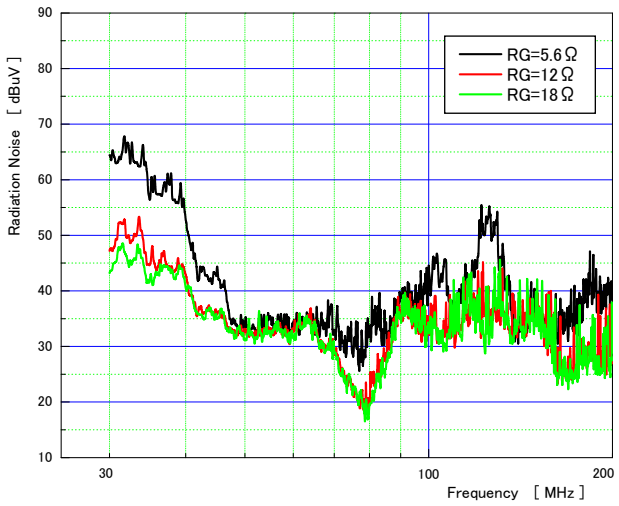
Amid the ongoing effort to comply with European CE marking for IGBT module-based converters, such as inverters and UPS, and with VCCI regulations in Japan, electromagnetic compatibility (EMC), particularly, holding down noise interferences (conductive and radiating noises emitted from devices in operation) to specifications or below, has become an essential aspect of circuit design.

As IGBT modules continue to offer enhanced characteristics, including faster switching and less loss, from generation to generation, high dv/dt and di/dt generated from their switching action is more frequently becoming a source of radiating noise interferences.

Radiation noises are primarily associated with harmonic LC resonance between stray capacitances, such as semiconductor device junction capacitances, and wiring stray inductances, triggered by high dv/dt and di/dt generated from the IGBTs during turn-on (reverse recovery of the FWD in the opposing arm).

Fig.4-14 shows examples of radiation noise of 1200V IGBT modules (2MBI150SC-120, 1200V, 150A). The radiation noise with twice standard gate resistance (12Ω) can decrease about 10dB or more.

A soft-waveform implementation of the switching characteristics to decrease radiation noises, however, tends to increase the switching loss. It is important to design the drive conditions to keep them balanced with the device operating conditions, module cooling conditions and other relevant conditions.



Motor driver:15kW, Molule:2MBI150SC-120

Fig. 4-14 Radiation noise of motor drivers

Moreover, a general example of countermeasures of radiation noise is shown in Table 4-2. Because the

generation factor and noise level are different according to the wiring structure of the device and the material and the circuit composition, etc., it is necessary to verify which of the countermeasures is effective.

Table 4-2 Countermeasures of radiation noise

Action	Description	Remarks
Review drive conditions (cut dv/dt and di/dt)	Increase the gate resistance (particularly, turn-on side) to two to thee times the standard value listed in the datasheet.	The switching loss increases. The switching time lengthens.
	Insert a small capacitor between the gate and emitter. Its capacitance should be somewhere from the feedback capacitance to the input capacitance (Cres to Cies).	The switching loss increases. The switching time lengthens.
Minimize the wiring between the snubber capacitor and the IGBT module	Minimize the wiring distance between the snubber capacitor and the IGBT module (connect to the module pins).	Also useful for canceling surge voltages during switching and dv/dt.
Cut wiring inductances	Use laminated bus bars to reduce inductances.	Also useful for canceling surge voltages during switching and dv/dt.
Filtering	Connect noise filters to device input and output.	Various filters are commercially available.
Shield wirings	Shield the I/O cables to cut radiating noise from the cables.	
Metalize the device case	Metalize the device cabinet to suppress noise emissions from the device.	

Chapter 5

Protection Circuit Design

CONTENTS

This section explains the protection circuit design.

1 Short circuit (overcurrent) protection

1-1 Short circuit withstand capability

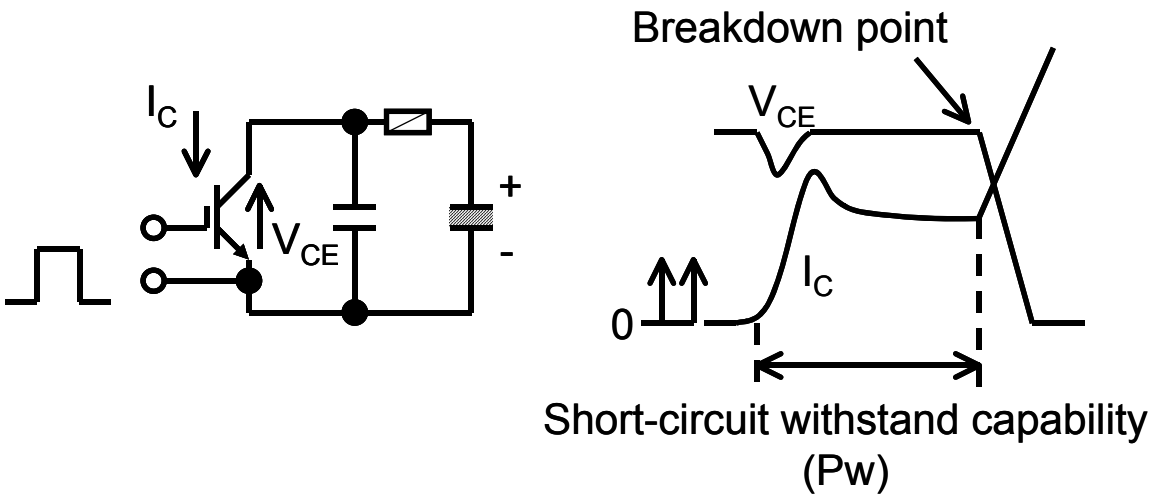
In the event of a short circuit, first the IGBT's collector current will rise, once it has reached a certain level, the C-E voltage will spike. Depending on the device's characteristics, during the short-circuit, the collector current can be kept at or below a certain level, however the IGBT will still continue to be subjected to a heavy load, that is, high voltage and high current. Therefore, this condition must be removed as soon as possible.

However, the amount of time allowed between the start of a short circuit until the current is cut off, is limited by the IGBT's short circuit withstand capability, which is determined by the amount of time, as illustrated in Fig. 5-1. The IGBT's short circuit withstand capability is defined as the start of the short-circuit current until the module is destroyed. Therefore, when the IGBT is short-circuited, large current is need to be cut off within the short circuit withstand capability.

The withstand capability depends on collector to emitter voltage V_{CE}, gate to emitter voltage V_{GE} and/or junction temperature T_j.

In general, , the larger supply voltage and/or the higher junction temperature are, the lower the withstand capability will be.

For more information on withstand capability, referred to the application manual or technical data.



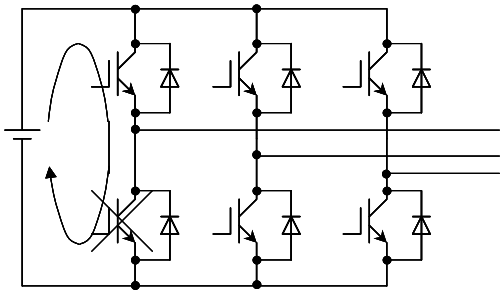
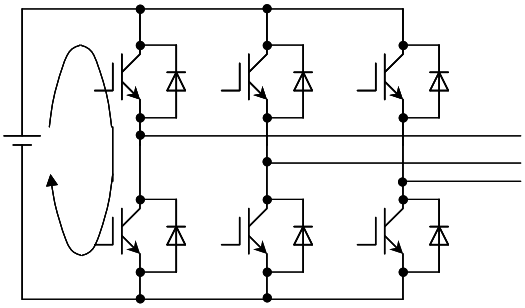
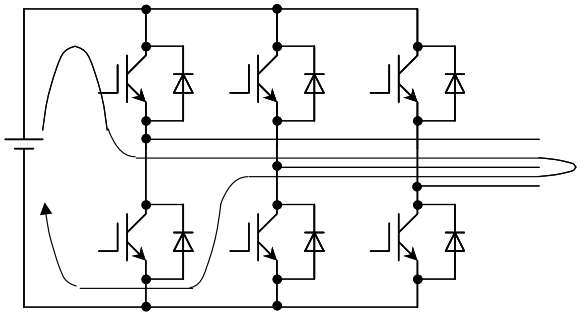
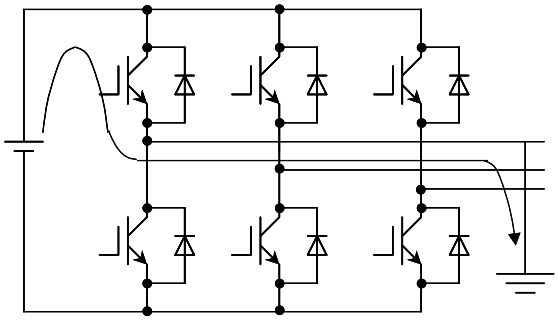
(a) Measuring circuit **(b) representative short-circuit waveform**

Fig. 5-1 Measuring circuit and waveform

1-2 Short-circuit modes and causes

Table 5-1 lists the short-circuit modes and causes that occur in inverters.

Table 5-1 Short circuit mode and cause

Short circuit mode	Cause
Arm short circuit 	Transistor or diode destruction
Series arm short circuit 	Faulty control/drive circuit or noise induce malfunction
Short in output circuit 	Miss wiring or dielectric breakdown of load
Ground fault 	Miss wiring or dielectric breakdown of load

1-3 Short-circuit (overcurrent) detection

1) Detection in the circuit

As described previously, in the event of a short-circuit, the IGBT must be protected as soon as possible. Therefore, the time from overcurrent detection to the complete turn-off in each circuit must work effectively as fast as possible.

Since the IGBT turns off very quickly, if the overcurrent is shut off using an ordinary drive signal, the collector-emitter voltage will rise due to the back-emf from parasitic inductances, and then the IGBT would have chance to be destroyed by overvoltage (RBSOA destructions). Therefore, it is recommended that when shutting off the overcurrent that the IGBT be turned off gently (Soft turn-off).

Figure 5-2 shows the insertion methods for overcurrent detectors, and Table 5-2 lists the features of the various methods along with their detection possibilities. After determining what kind of protection is necessary, select the most appropriate form of detection.

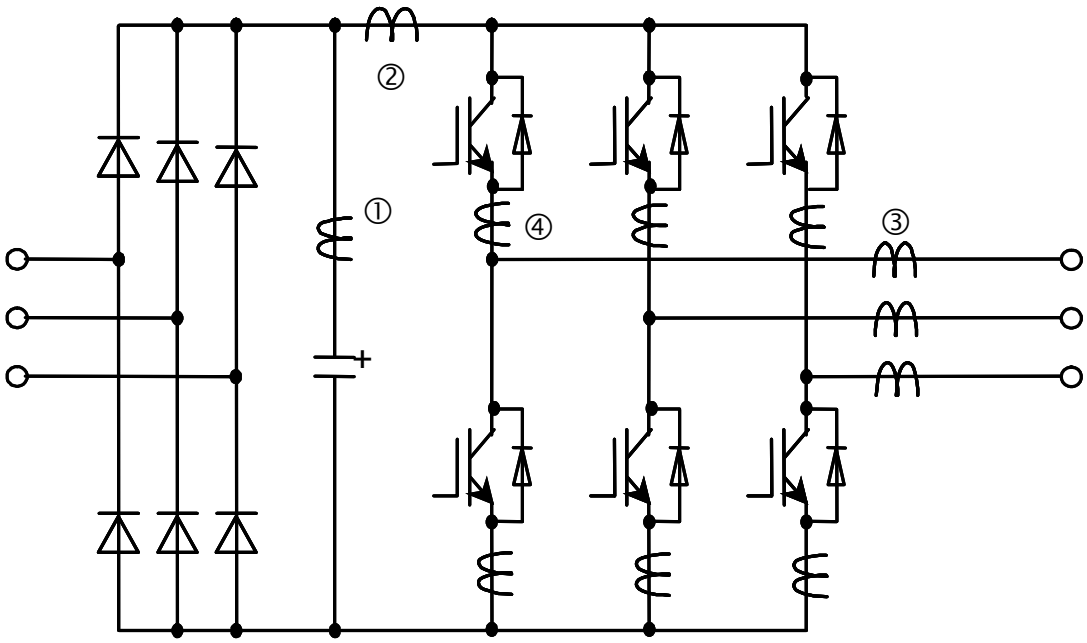


Fig. 5-2 Overcurrent detector insertion methods

Table 5-2 Overcurrent detector insertion positions and function

Detector insertion position	Features	Detection function
Insertion in line with smoothing capacitor Fig.5-2/①	• AC current transformer available • Low detection precision	• Arm short-circuit • Short in output circuit • Series arm short-circuit • Ground fault
Insertion at inverter input Fig.5-2/②	• Necessary to use DC current transformer • Low detection precision	• Arm short-circuit • Short in output circuit • Series arm short-circuit • Ground fault
Insertion at inverter output Fig.5-2/③	• AC current transformer available for high frequency output equipment • High detection precision	• Short in output circuit • Ground fault
Insertion in line with switches Fig.5-2/④	• Necessary to use DC current transformer • High detection precision	• Arm short-circuit • Short in output circuit • Series arm short-circuit • Ground fault

2) Detecting using $V_{CE(sat)}$

This method has a feature of protection against all possible short-circuit types listed in Table5-1. Since all operations from overcurrent detection to protection are done on the drive circuit side, the fastest protection is possible. A short-circuit protection schematic, based in $V_{CE(sat)}$ detection, is shown in Fig.5-3.

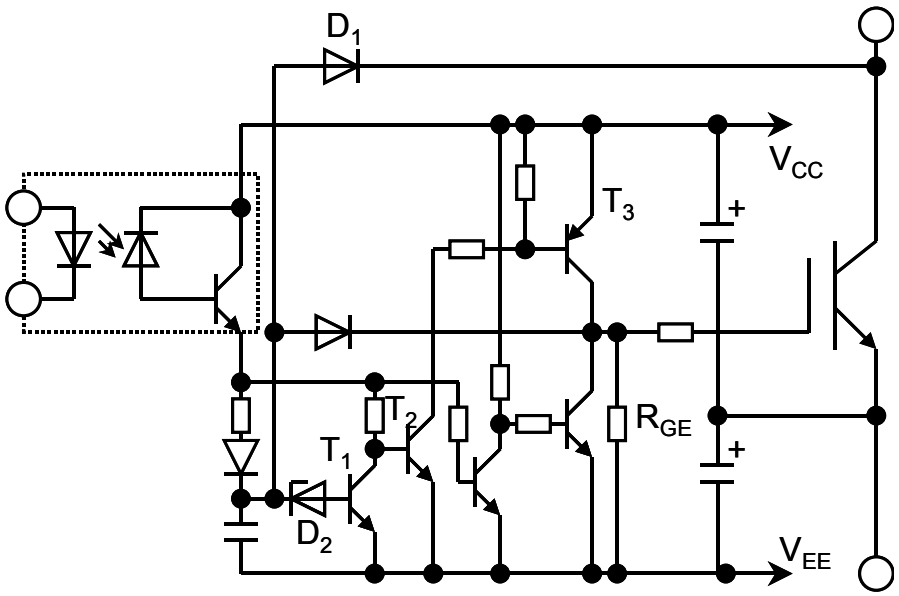
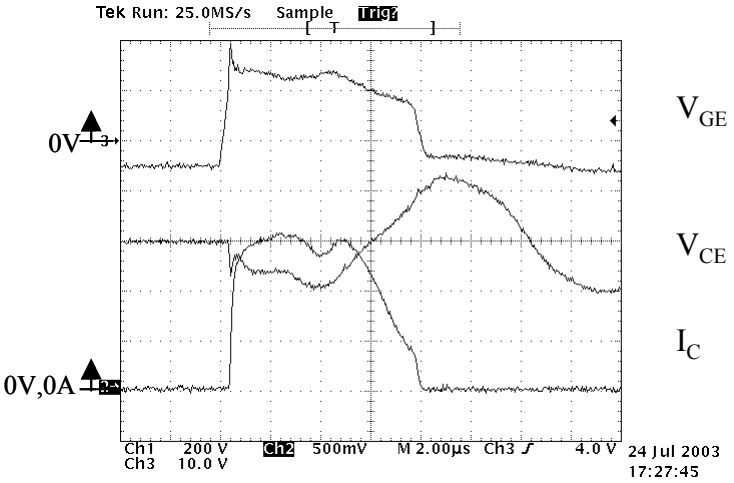


Fig. 5-3 Short-circuit protection schematic based in VCE(sat) detection

This circuit uses D_1 to constantly monitor the collector-emitter voltage, so if during operation the IGBT's collector-emitter voltage rises above the limit at D_2, then a short-circuit condition will be detected and T1 will be switched on while T_2 and T_3 are switched off. At this time, the accumulated charge at the gate is slowly released through the R_{GE}, so a large voltage spike is prevented when the IGBT is turned off. Gate driver hybrid IC_S (model VLA517) have similar kind of protective circuit built in, thereby simplifying the drive circuit design. For more details, refer to Chapter 7 "Drive Circuit Design". Fig. 5-4 shows an example of IGBT waveforms in short circuit protection.



2MBI300UD-120

Ed=600V, V_{GE}=+15V, –5V (VLA517), R_G=3.3Ω, Tj=125°C

V_{CE}=200V/div, I_C=250A, V_{GE}=10V/div, t=2µs/div

Fig. 5-4 Waveforms during short circuit protection

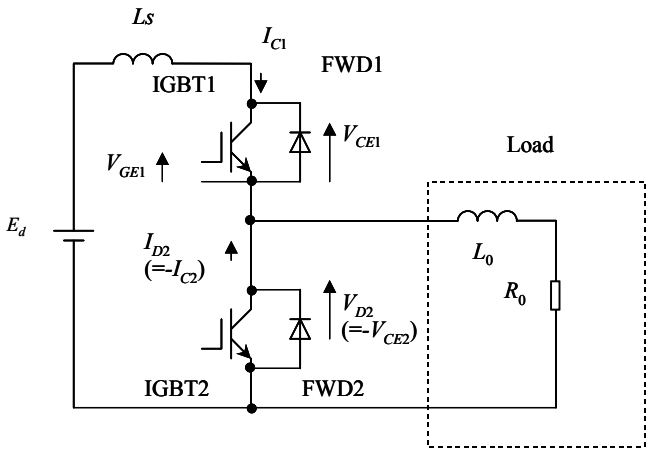
2 Overvoltage protection

2.1 Overvoltage causes and their suppression

1) Overvoltage causes

Due to the fast switching feature of IGBTs at turn-off and/or during FWD reverse recovery, the instantaneous rate in current over time (di/dt) would have very high value. Therefore the parasitic inductances to the module would produce a high turn-off surge voltage (V=L(di/dt)).

In this section, an example of solutions both for IGBT and FWD are described with explanation of the root causes and practical methods to suppress the surge voltage with typical IGBT waveforms at turn-off To demonstrate the turn-off surge voltage, a simplified chopper circuit and the IGBT turn-off voltage and current waveforms are shown in Fig. 5-5 and 5-6, respectively.



E_d: DC supply voltage, L_S: Main circuit parasitic inductance, Load:L_0,R_0

Fig. 5-5 Chopper circuit

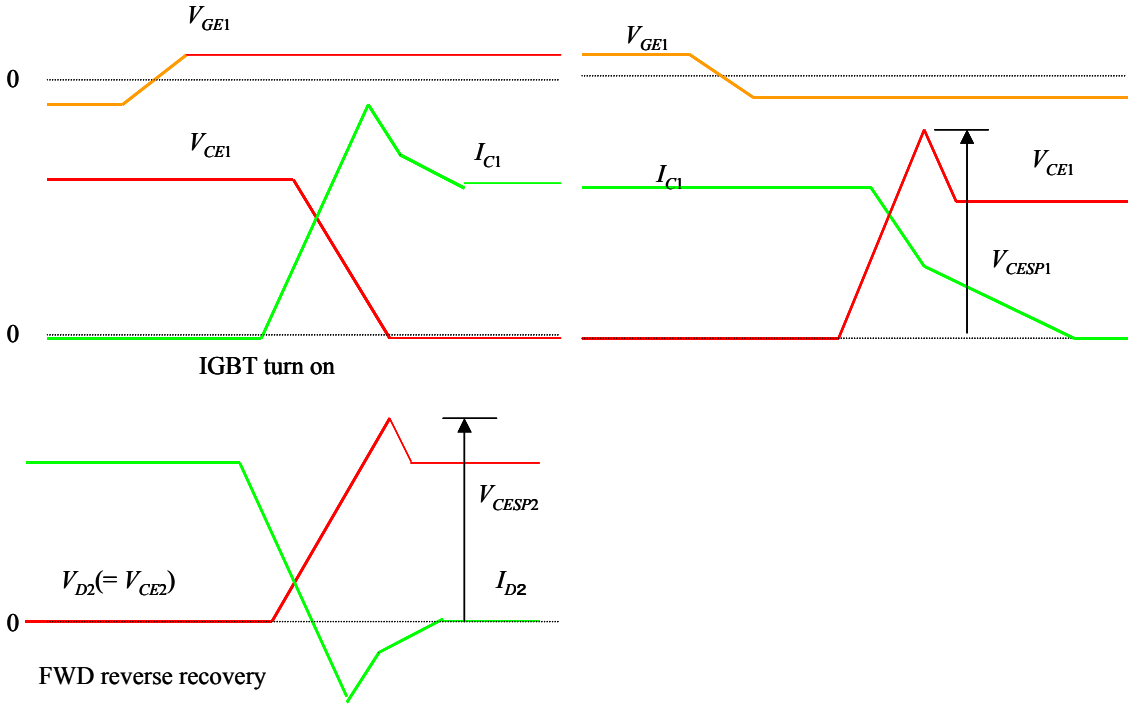


Fig. 5-6 Switching waveforms

The turn-off surge voltage peak V_{CESP} can be calculated as follows:

$$V_{CESP} = Ed + (-L_S \bullet dIc/dt) \cdots\cdots\cdots\cdots\cdots\cdots \text{①}$$

dIc/dt: Instantaneous rate in current over time

If V_{CESP} exceeds the maximum C-E (V_{CES}) rating of IGBT, IGBT module would be destroyed.

2) Overvoltage suppression methods

Several methods for suppressing the turn-off surge voltage, the cause for overvoltage, are listed below:

a. Control the surge voltage with an additional protection circuit (snubber circuit) to the IGBT.
   A film capacitor in the snubber circuit, which is connected as close as possible to the IGBT, works to bypass the high frequency surge currents.
b. Adjust the IGBT drive circuit's $-V_{GE}$ and/or R_G in order to reduce the di/dt value. (Refer to Chapter 7, "Drive Circuit Design".)
c. Place the electrolytic capacitor as close as possible to the IGBT in order to reduce the parasitic inductance of the wiring. A low impedance capacitors have better effect.
d. To reduce the inductance of the main circuit as well as the snubber circuit parasitic inductances, thicker and shorter connections are recommended. Laminated bus bars are best solution to reduce parasitic inductances.

2.2 Types of snubber circuits and their features

Snubber circuits can be classified into two types: individual and lump. Individual snubber circuits are connected to each IGBT, while lump snubber circuits are connected between the DC power-supply bus and the ground for centralized protection.

1) Individual snubber circuits

Examples of typical individual snubber circuits are listed below.

a) RC snubber circuit
b) Charge and discharge RCD snubber circuit
c) Discharge-suppressing RCD snubber circuit

Table 5-3 shows the schematic of each type of individual snubber circuit, its features, and an outline of its main applications.

2) Lump snubber circuits

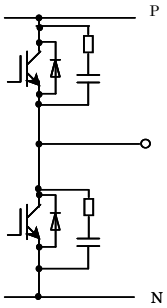
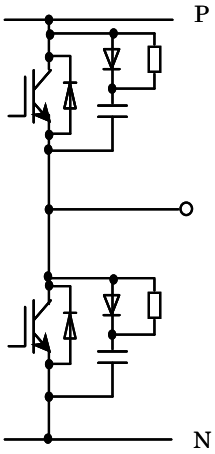
Examples of typical snubber circuits are listed below.

a) C snubber circuits
b) RCD snubber circuits

Lump snubber circuits are becoming increasingly popular due to circuit simplification.

Table 5-4 shows the schematic of each type of lump snubber circuit, its features, and an outline of its main applications. Table 5-5 shows the capacity selection of a C type snubber circuit. Fig. 5-7 shows the current and voltage turn-off waveforms for an IGBT connected to a lump snubber circuit.

Table 5-3 Individual snubber circuits

Snubber circuit schematic	Circuit features (comments)	Main application
RC snubber circuit  	• Very effective on turn-off surge voltage suppression • Best for chopper circuits • For high power IGBTs, the low resistance snubber resistance is necessary, which results increase in turn-off collector current and higher IGBT load.	Welding Switching power supply
Charge and discharge RCD snubber circuit  	• The moderate effect in turn-off surge voltage suppression. • In contrast to the RC snubber circuit, additional snubber diodes connected paralley to the snubber resistance.. This diode enable not to use low snubber resistance. consequently preventing the IGBT higher load turn-on issue in RC snubber solution above. • Since the power dissipation of the snubber circuit (primarily caused by the snubber resistance) is much higher than that of a discharge suppressing snubber circuit below, it is not considered suitable for high frequency switching applications. • The power dissipation caused by the resistance of this circuit can be calculated as follows: $P = \frac{L \bullet Io^2 \bullet f}{2} + \frac{C_S \bullet Ed^2 \bullet f}{2}$ L: Parasitic inductance of main circuit, Io: Collector current at IGBT turn-off, Cs: Capacitance of snubber capacitor, Ed: DC supply voltage, f :Switching frequency	

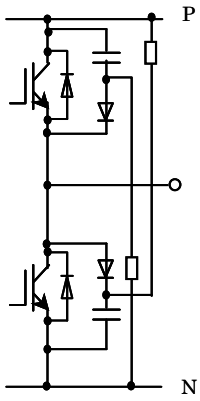
Discharge suppressing RCD snubber circuit  	• Limited effect on turn-off surge voltage suppression • Suitable for high-frequency switching • Small power dissipation of snubber circuit i. • The power dissipation caused by the resistance of this circuit can be calculated as follows: $P = \frac{L \bullet Io^2 \bullet f}{2}$ L: Parasitic inductance of main circuit Io: Collector current at IGBT turn-off f :Switching frequency	Inverter

Table 5-4 Lump snubber circuits

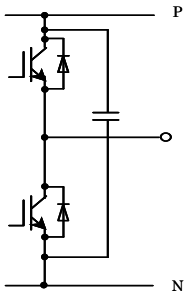
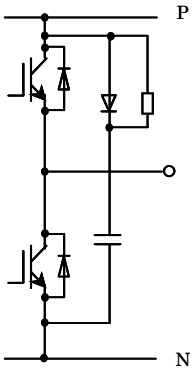
Snubber circuit schematic	Circuit features (comments)	Main application
C snubber circuit  	• The simplest topology. • The LC resonance circuit, which consists of a main circuit parasitic inductance and snubber capacitor, may have a chance of the C-E voltage oscillation.	Inverter
RCD snubber circuit  	• In case inappropriate snubber diode is used, a high spike voltage and/or the output voltage oscillation in the diodes reverse recovery would be observed	Inverter

Table 5-5 Guidelines for designing the lump C snubber circuit capacitance

Item / Module rating		Drive conditions[*1]		Main circuit wiring inductance (μH)	Snubber capacitance Cs (μF)
		$-V_{GE}$(V)	R_G(Ω)		
600V	50A	max 15V	min.43Ω	-	0.47μF
	75A		min.30 Ω		
	100A		min.13 Ω		
	150A		min.9 Ω	max 0.20μH	1.5 μF
	200A		min.6.8 Ω.	max.0.16 μH	2.2 μF
	300A		min.4.7 Ω	max.0.10 μH.	3.3 μF
	400A		min.6.0 Ω	max.0.08 μH.	4.7 μF
1200V	50A	max 15V	min.22 Ω	-	0.47 μF
	75A		min.4.7 Ω		
	100A		min.2.8 Ω		
	150A		min.2.4 Ω	max.0.20 μH.	1.5 μF
	200A		min.1.4 Ω	max.0.16 μH.	2.2 μF
	300A		min.0.93 Ω	max.0.10 μH.	3.3 μF

*[1]: Typical external gate resistance of V series IGBT are shown.

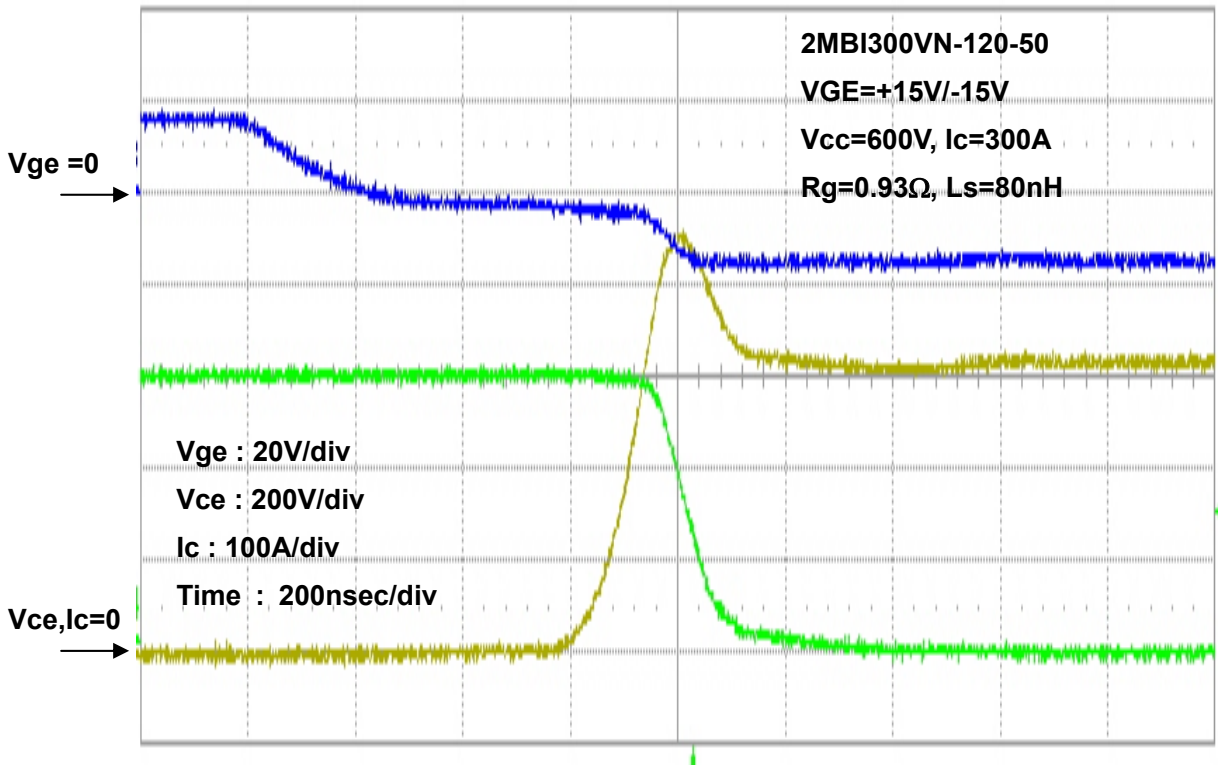


Fig. 5-7 Current and voltage waveforms of IGBT with lump snubber circuit at turn-off

2-3 Discharge-suppressing RCD snubber circuit design

The discharge suppressing RCD can be considered the most suitable snubber circuit for IGBTs. Basic design methods for this type of circuit are explained in the following.

1) Study of applicability

Figure 5-8 is the turn-off locus waveform of an IGBT in a discharge-suppressing RCD snubber circuit. Fig. 5-9 shows the IGBT current and voltage waveforms at turn-off.

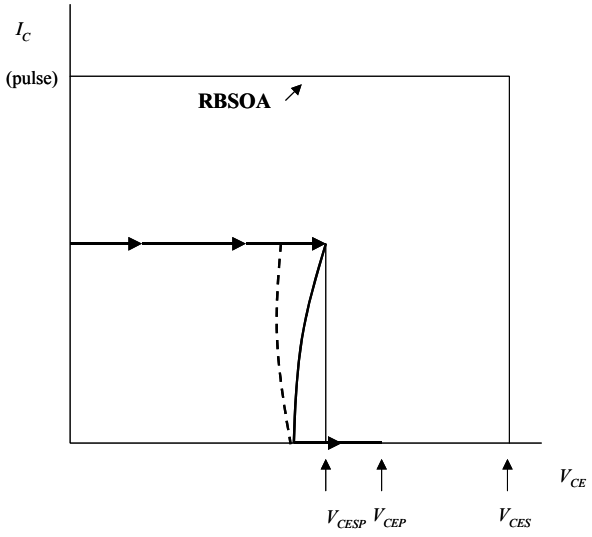


Fig. 5-8 Turn-off locus waveform of IGBT

The discharge-suppressing RCD snubber circuit is activated when the IGBT C-E voltage starts to exceed the DC supply voltage. The dotted line in diagram Fig. 5-8 shows the ideal operating locus of an IGBT. In an actual application, the wiring inductance of the snubber circuit or a transient forward voltage drop in the snubber diode can cause a spike voltage at IGBT turn-off. This spike voltage causes the sharp-cornered locus indicated by the solid line in Fig. 5-8.

The discharge-suppressing RCD snubber circuits applicability is decided by whether or not the IGBTs operating locus is within the RBSOA at turn-off.

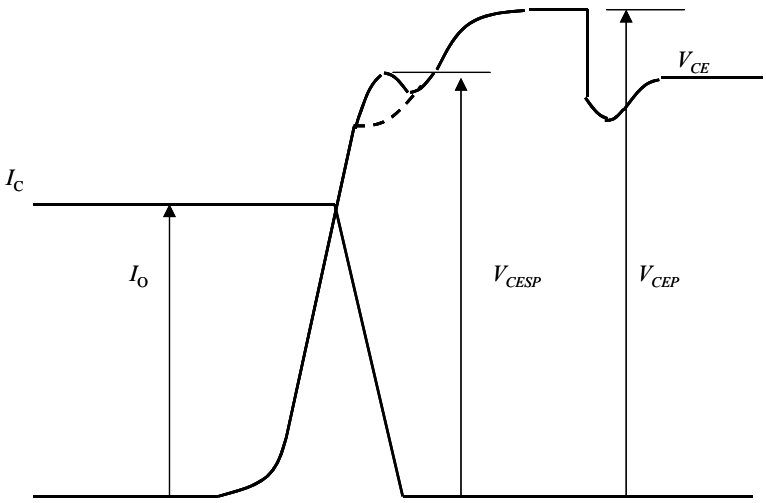


Fig. 5-9 Voltage and current waveforms at turn-off

The spike voltage at IGBT turn-off is calculated as follows:

$$V_{CESP} = Ed + V_{FM} + (-L_S \bullet dIc/dt) \quad \cdots\cdots\cdots\cdots ②$$

Ed: Dc supply voltage
V_{FM}: Transient forward voltage drop in snubber diode
The reference values for the transient forward voltage drop in snubber diodes is as follows:
600V class: 20 to 30V
1200V class: 40 to 60V
Ls: Snubber circuit wiring parasitic inductance
dIc/dt: The instantaneous rate in collector current over time in IGBT turn-off

2) Calculating the capacitance of the snubber capacitor (Cs)

The minimum capacitance of a snubber capacitor is calculated as follows:

$$C_S = \frac{L \bullet Io^2}{(V_{CEP} - Ed)^2} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots ③$$

L: Main circuit wiring parasitic inductance
Io: Collector current at IGBT turn-off
VCEP: Snubber capacitor peak voltage
Ed: DC supply voltage

VCEP must be lower than IGBT C-E breakdown voltage. High frequency capacitors such as film capacitors are recommended.

3) Calculating Snubber resistance (Rs)

The function required of snubber resistance is to discharge the electric charge accumulated in the snubber capacitor before the next IGBT turn-off event.

To discharge 90% of the accumulated energy by the next IGBT turn-off event, the snubber resistance must be as follows:

$$R_S \leq \frac{1}{2.3 \bullet C_S \bullet f} \quad \cdots\cdots ④$$

f: Switching frequency

If the snubber resistance is set too low, the snubber circuit current will oscillate and the peak collector current at the IGBT turn-off will increase. Therefore, set the snubber resistance in a range below the value calculated in the equation.

Independently to the resistance, the power dissipation loss P (Rs) is calculated as follows:

$$P(R_S) = \frac{L \bullet Io^2 \bullet f}{2} \quad \cdots\cdots ⑤$$

4) Snubber diode selection

A transient forward voltage drop in the snubber diode is one factor that would cause a spike voltage at IGBT turn-off.

If the reverse recovery time of the snubber diode is too long, then the power dissipation loss will also be much greater during high frequency switching. If the snubber diode's reverse recovery is too hard, then the IGBT C-E voltage will drastically oscillate.

Select a snubber diode that has a low transient forward voltage, short reverse recovery time and a soft recovery.

5) Snubber circuit wiring precautions

The snubber circuit's wiring inductance is one of the main causes of spike voltage, therefore it is important to design the circuit with the lowest inductance possible.

2-4 Example of characteristic of spike voltage

The spike voltage shows various behaviors depending on the operation, drive and circuit conditions. Generally, the spike voltage becomes higher when the collector voltage is higher, the circuit inductance is larger, and the collector current is larger. As an example of spike voltage characteristic, the current dependence of spike voltage at IGBT turn-off and FWD reverse recovery is shown in Figure 5-10.

As this figure shows, the spike voltage at IGBT turn-off becomes higher when the collector current is higher, but the spike voltage at FWD reverse recovery becomes higher when the current is low. Generally, the spike voltage during reverse recovery becomes higher when the collector current is in the low current area that is a fraction of the rated current.

The spike voltage shows various behaviors depending on the operation, drive and circuit conditions. Therefore, make sure that the current and voltage can be kept within the RBSOA described in the specification in any expected operating condition of the system.

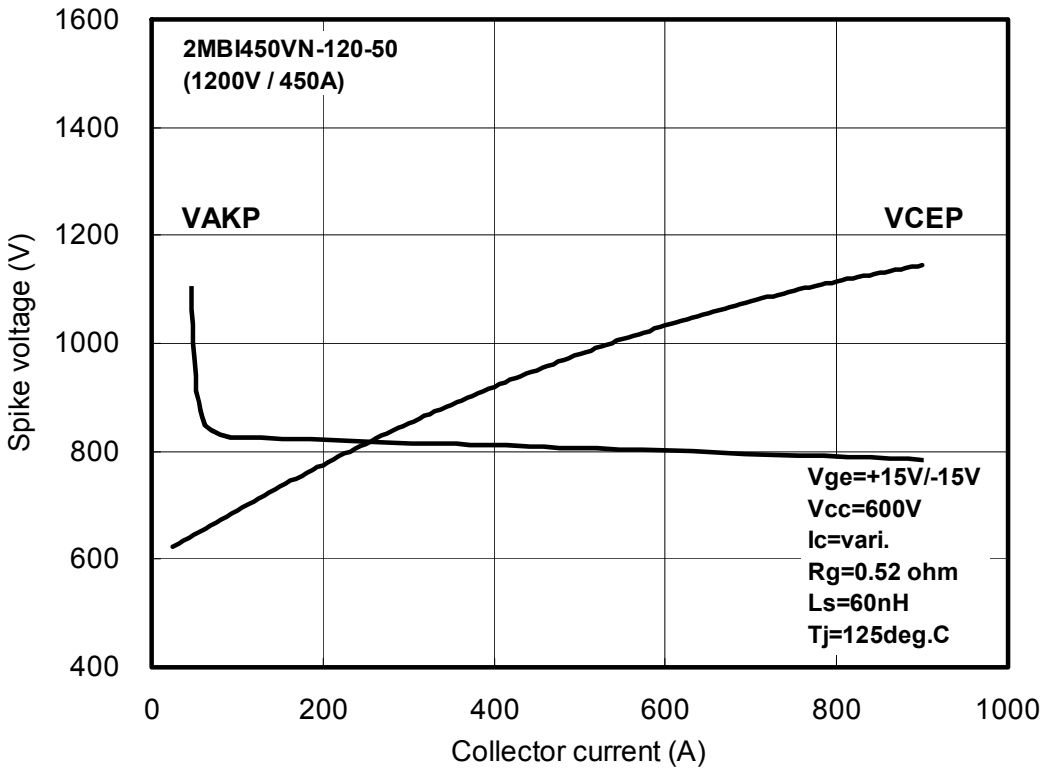


Fig. 5-10 Spike voltages dependency on collector current

2-5 Spike voltage suppression circuit - clamp circuit -

In general, spike voltage generated between collector to emitter can be suppressed by means of decreasing the stray inductance or installing snubber circuit. However, it may be difficult to decrease the spike voltage under the hard operating conditions.

For this case, it is effective to install the active clamp circuits, which is one of the spike voltage suppressing circuits.

Fig. 5-11 shows the example of active clamp circuits.

In the circuits, Zenner diode and a diode connected with the anti-series in the Zenner diode are added.

When the Vce over breakdown voltage of Zenner diode is applied, IGBT will be turned-off with the similar voltage as breakdown voltage of Zenner diode. Therefore, installing the active clamp circuits can suppress the spike voltage.

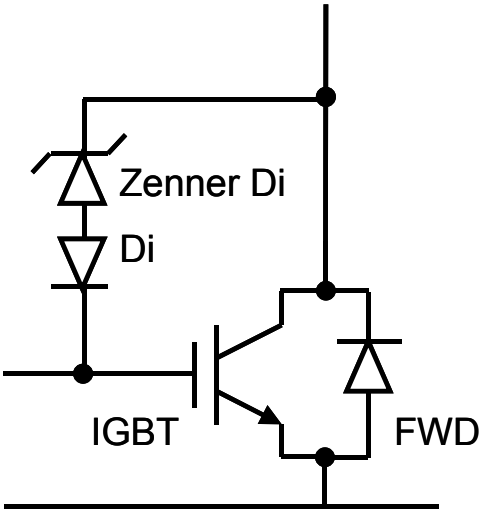


Fig. 5-11 Active clamp circuit

Moreover, avalanche current generated by breakdown of Zenner diode, charge the gate capacitance so as to turn-on the IGBT. As the result, di/dt at turn-off become lower than that before adding the clamp circuit (Refer to Fig. 5-12). Therefore, because switching loss may be increased, apply the clamp circuit after various confirmations for design of the equipment.

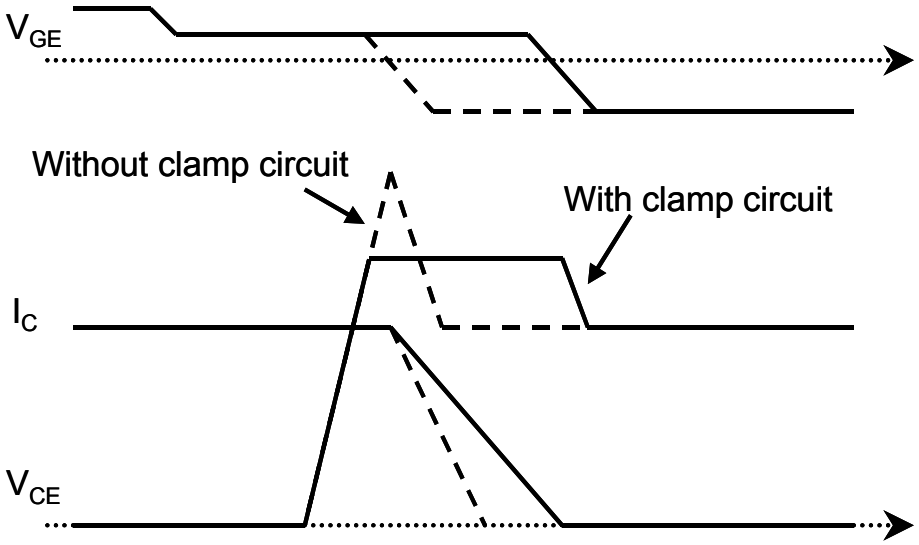


Fig. 5-12 Schematic waveform for active clamp circuit

Chapter 6

Cooling Design

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This section explains the cooling design.

For safe IGBT operation, the junction temperature (Tj) must never exceed Tj(max). Therefore, it is necessary to have a cooling design capable of keeping the junction temperature below Tj(max), even during overload conditions.

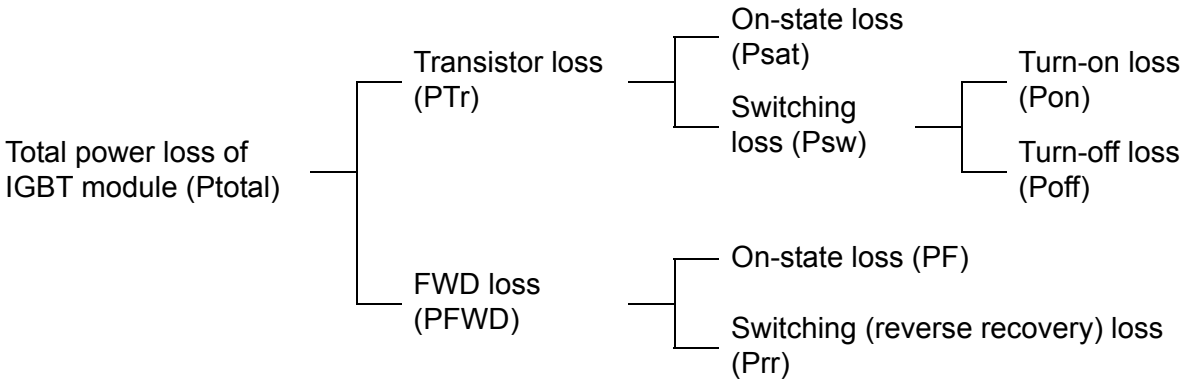
1 Power dissipation loss calculation

In this section, the simplified methods of calculating power dissipation for IGBT modules are explained. However, the detailed calculation tool of IGBT simulator is available on the Fuji Electric WEB site. It helps to calculate the power dissipation and thermal design for various working condition of various Fuji IGBT modules.

1-1 Types of power loss

An IGBT module consists of IGBT chips and FWD chips. The sum of the power losses from these sections equals the total power loss for the module. Power loss can be classified as either on-state loss or switching loss. A diagram of the power loss factors is shown as follows.

Power loss factors



The on-state power loss from the IGBT and FWD sections can be calculated using the output characteristics, while switching loss can be calculated from switching loss vs. collector current characteristics. Use these power loss calculations in order to design cooling sufficient to keep the junction temperature Tj below the maximum rated value.
The on-voltage and switching loss values to be used here, are based on the typical junction temperature Tj (125°C or 150°C are recommended).
For characteristics data, refer to the module specification sheets.

1-2 DC chopper circuit power loss calculations

For easy approximate calculations, consider the current flowing to the IGBT or FWD as a train of square waves. Fig.6-1 is a diagram showing the approximate waveforms of a DC chopper circuit. At collector current Ic the saturation voltage is represented by $V_{CE(sat)}$ and switching energy is represented by Eon and Eoff. At FWD forward current I_F, V_F represents the on- voltage and E_{RR} represents the energy loss during reverse recovery. Using the above parameters, IGBT power loss can be calculated as follows:

IGBT power dissipation loss (w) = On-state loss + Turn-on loss + Turn-off loss

$$= \left[t1/t2 \times V_{CE(sat)} \times I_C\right] + \left[fc \times \left(E_{on} + E_{off}\right)\right]$$

FWD power dissipation loss (w) = On-state loss + Reverse recovery loss

$$= \left[\left(1 - \left(t1/t2\right)\right) \times I_F \times V_F\right] + \left[fc \times E_{rr}\right]$$

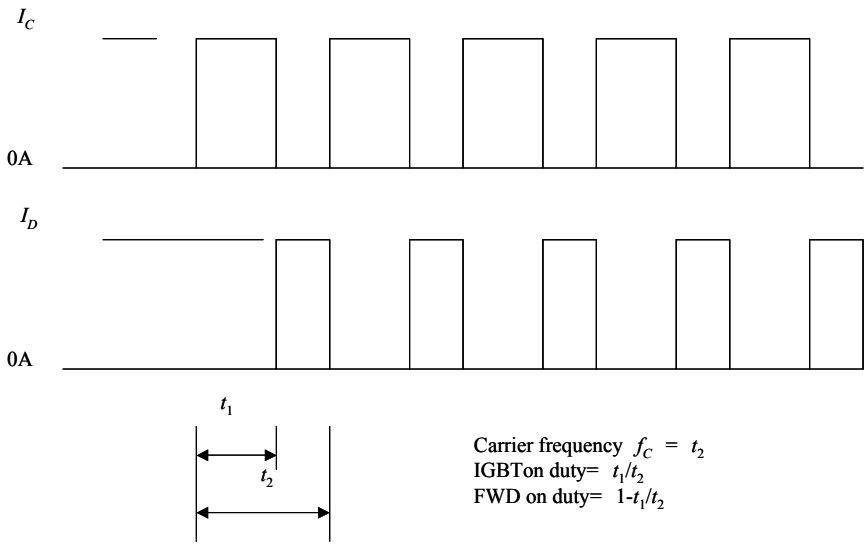


Fig. 6-1 DC chopper circuit current waveforms

The DC supply voltage, gate resistance, and other circuit parameters, may deviate from the standard value listed in the module specification sheets. In this event, approximate values can be calculated according to the following rules:

- DC supply voltage Ed(VCC) deviation
  On voltage: Not dependent on Ed(VCC)
  Switching loss: Proportional to Ed(VCC)

- Gate resistance deviation
  On voltage: Not dependent on gate resistance
  Switching loss: Proportional to switching time and dependent on gate resistance

1-3 Sine-wave VVVF inverter application power dissipation loss calculation

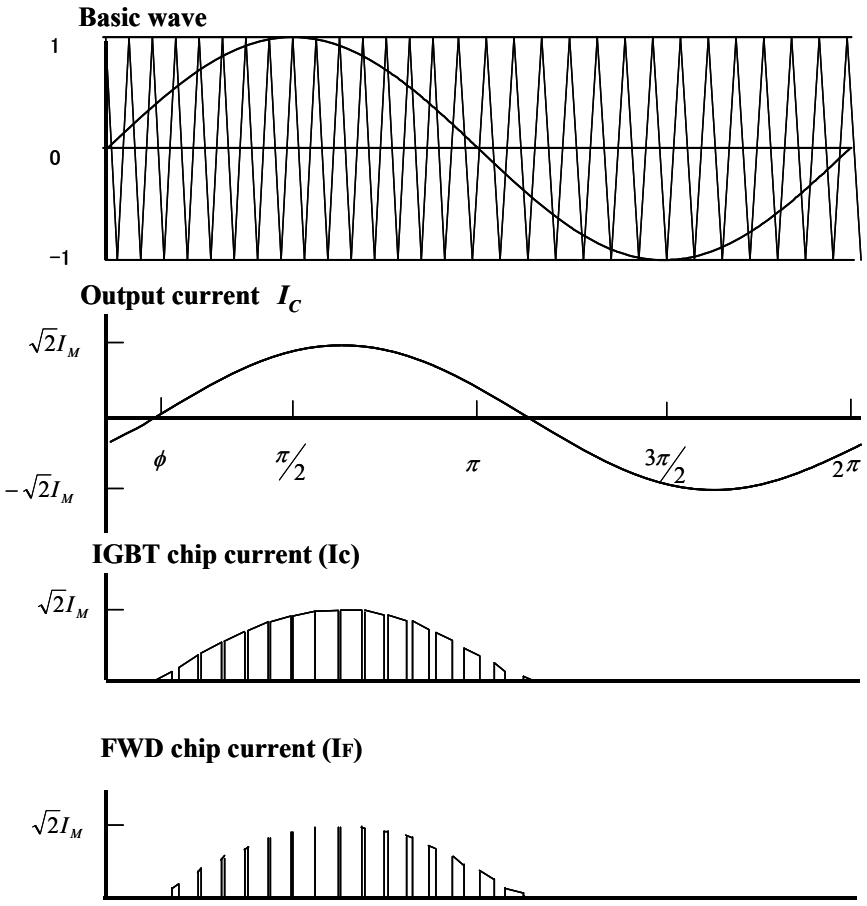


Fig. 6-2 PWM inverter output current

When using a VVVF inverter for a PWM control, the current value and operation keep changing as shown in Fig.6-2. Therefore, it is necessary to use computer simulations in order to make detailed power loss calculations. However, since computer simulations are very complicated, the following is an explanation of a simple method that generates approximate values.

Prerequisites

For approximate power loss calculations, the following prerequisites are necessary:
- Three-phase PWM-control VVVF inverter for sine-wave current output
- PWM control based on the comparison of sine-waves and sawtooth waves
- Output current in ideal sine-wave form

Calculating on-state power loss (Psat, P_F)

As displayed in Fig.6-3, the output characteristics of the IGBT and FWD have been approximated based on the data contained in the module specification sheets.

On-state power loss in IGBT chip (P_{sat}) and FWD chip (P_F) can be calculated as follows:

$$(P_{sat}) = DT\int_0^x I_C V_{CE(sat)} d\theta$$
$$= \frac{1}{2} DT\left[\frac{2\sqrt{2}}{\pi} I_M V_O + I_{M^2} R\right]$$

$$(P_F) = \frac{1}{2} DF\left[\frac{2\sqrt{2}}{\pi} I_M V_O + I_{M^2} R\right]$$

DT, DF: Average conductivity of the IGBT and FWD at a half wave of the output current. (Refer to Fig.6-4)

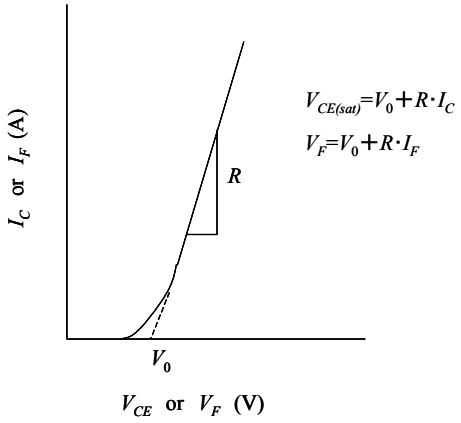


Fig. 6-3 Approximate output characteristics

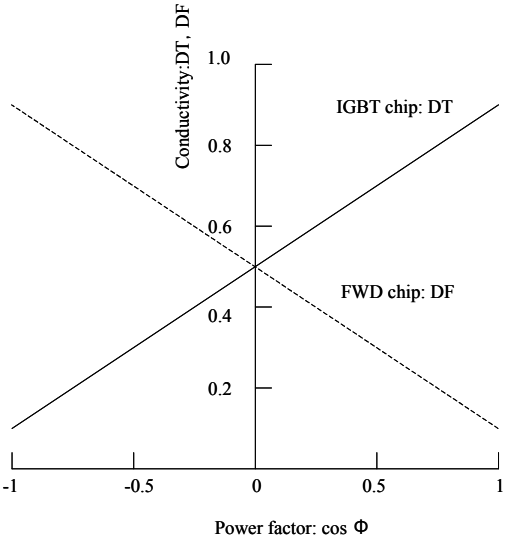


Fig. 6-4 Relationship between power factor sine-wave PWM inverter and conductivity

Calculating switching loss

The characteristics of switching loss vs. I_C are generally approximated using the following equations and Fig.6-5 (Module specification sheet data).

$$E_{on} = E_{on'}\left(I_C / ratedI_C\right)^a$$

$$E_{off} = E_{off'}\left(I_C / ratedI_C\right)^b$$

$$E_{rr} = E_{rr'}\left(I_C / ratedI_C\right)^c$$

a, b, c: Multiplier
Eon', Eoff', Err': Eon, Eoff and Err at rated IC

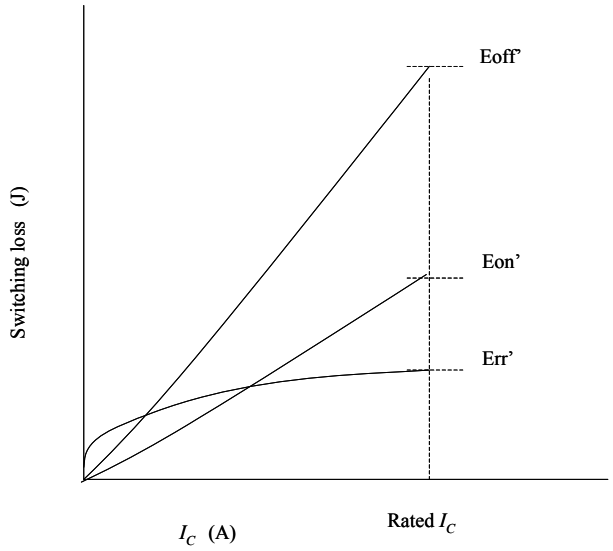


Fig. 6-5 Approximate switching losses

The switching loss can be represented as follows:

• Turn-on loss (P_{on})

$$P_{on} = fo\sum_{K=1}^{n}\left(E_{on}\right)k \qquad \left(n: Half-cycle\ switching\ count = \frac{fc}{2fo}\right)$$

$$= foE_{on}'\frac{1}{rated\ I_{C^a}}\sum_{k=1}^{n}\left(I_{C^a}\right)k$$

$$= foE_{on}'\frac{n}{rated\ I_{C^a}\times\pi}\int_0^{\pi}\sqrt{2}I_{M^a}\sin\theta d\theta$$

$$\fallingdotseq foE_{on}'\frac{1}{rated\ I_{C^a}}nI_{M^a}$$

$$= \frac{1}{2}fcE_{on}'\left[\frac{I_M}{rated\ I_C}\right]^a$$

$$= \frac{1}{2}fcE_{on}\left(I_M\right)$$

$E_{on}(IM)$:Ic= E_{on} at I_M

• Turn-off loss (P_{off})

$$P_{off} \fallingdotseq \frac{1}{2}fcE_{off}\left(I_M\right)$$

$E_{off}(I_M)$:Ic= E_{off} at I_M

• **FWD reverse recovery loss (P_{rr})**

$$P_{off} \fallingdotseq \frac{1}{2} fcE_{rr}(I_M)$$

$E_{rr}(I_M)$:I_c= E_{rr} at I_M

Calculating total power loss

Using the results obtained in section 1.3 subsection 2 and 3.

IGBT chip power loss: $P_{Tr} = P_{sat} + P_{on} + P_{off}$

FWD chip power loss: $P_{FWD} = P_F + P_{rr}$

The DC supply voltage, gate resistance, and other circuit parameters will differ from the standard values listed in the module specification sheets.
Nevertheless, by applying the instructions of this section, the actual values can easily be calculated.

2 Selecting heat sinks

Most of power diodes, IGBTs, transistors and other power devices are designed to have high voltage isolation between electrodes and base plate. This type of module can be mounted and compactly connected in a variety of equipment, because multiple devices can be mounted on a single heat sink. However, in order to ensure safe operation, the power loss (heat) generated from each module must be transferred efficiently. This is the reason why heat sink selections are very important. The basic of heat sink selection will be described in the following sections.

2-1 Thermal equations for on-state power loss calculations

The heat conduction of a power semiconductor can be simulated as an electric circuit. For this example, only one IGBT module is mounted on the heat sink, the equivalent circuit is shown in Fig.6-6

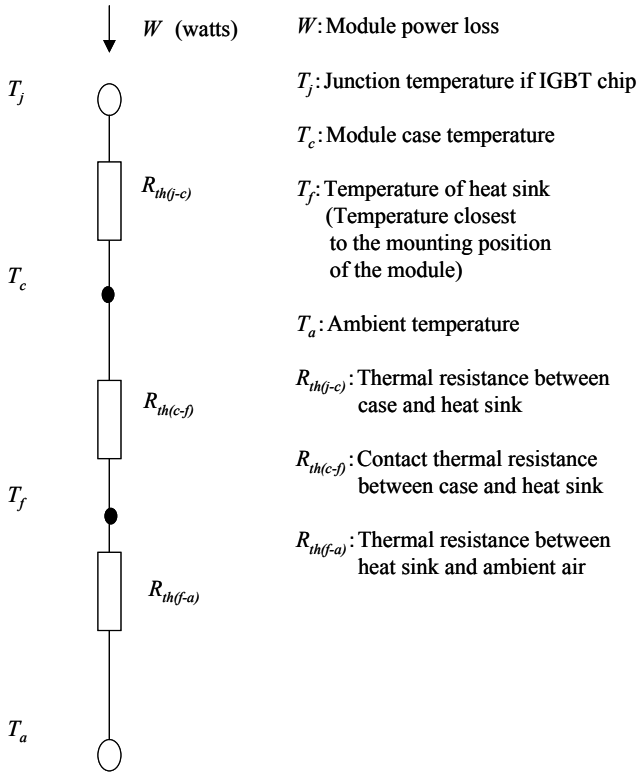


Fig. 6-6 Thermal resistance equivalent circuit

Using the above equivalent circuit, the junction temperature (Tj) can be calculated using the following thermal equation:

$$Tj = W \times \{Rth(j-c) + Rth(c-f) + Rth(f-a)\} + Ta$$

Note that the case temperature (T_c) and heat sink surface temperature mentioned here are measured from the base plate of the IGBT module directly underneath the chip. As shown in Fig.6-7, the temperature at all other points may be low due to the heat spreading of the heat sink, and this needs to be taken into consideration in final heat sink selection. Next, the equivalent circuit of an IGBT (2-pack-module) and a diode bridge mounted on a heat sink is shown in Fig.6-8. The thermal equations in this case are as follows:

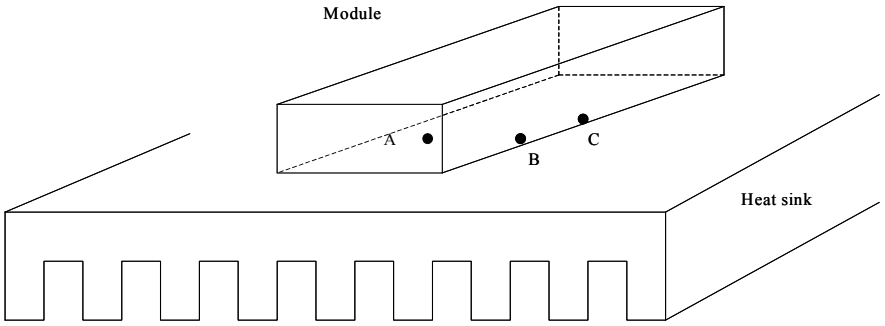
$$Tj(d) = Wd \times [Rth(j-c)d + Rth(c-f)d] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$

$$Tj(T) = WT \times Rth(j-c)T + [(WT + WD) \times Rth(c-f)T] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$

$$Tj(D) = WD \times Rth(j-c)D + [(WT + WD) \times Rth(c-f)T] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$

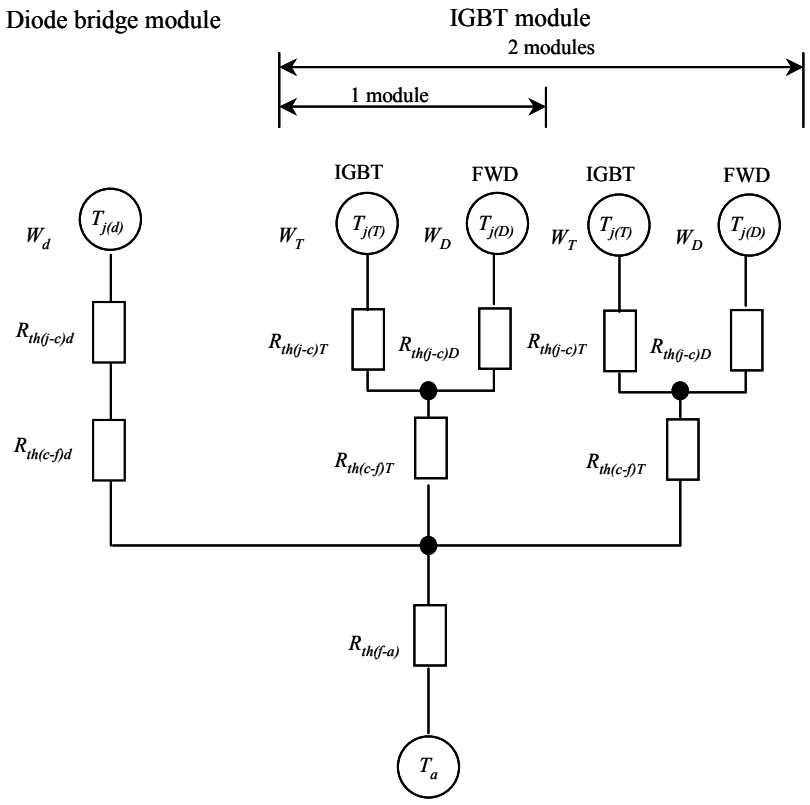
Use the above equations in order to select a heat sink that can keep the junction temperature (T_j) below T_j(max).

A : Directly below the chip by the case
B : Base, 14mm from point A
C : Base, 24mm from point A



	Point A	Point B	Point C
T_C (°C)	51.9	40.2	31.4
T_f (°C)	45.4	36.9	30.2

Fig. 6-7 Example of case and heat sink temperature measurement



W_d, $T_{j(d)}$, $R_{th(\ )d}$: Diode bridge (For one module)
W_T, $T_{j(T)}$, $R_{th(\ )T}$: IGBT (Each element)
W_D, $T_{j(D)}$, $R_{th(\ )D}$: FWD (Each element)

Fig. 6-8 Thermal resistance equivalent circuit

2-2 Thermal equations for transient power loss calculations

In general, as described above steady-state T_j calculation provides enough information for heat sink design, however, actual operation has temperature ripples as shown in Fig.6-10 because repetitive switching produce pulse wave power dissipation and heat generation.

First consider the power loss as a train of constant cycles, and constant-peak square pulses. Then calculate the approximate peak of the temperature ripples using the transient thermal impedance curve given in the module specification sheets.

Be certain to select a heat sink that will also keep the T_{jp} below T_j (max).

$$Tjp - T_C = P \times \left[R(\infty) \times \frac{t1}{t2} + \left(1 - \frac{t1}{t2}\right) \times R(t1+t2) - R(t2) + R(t1) \right]$$

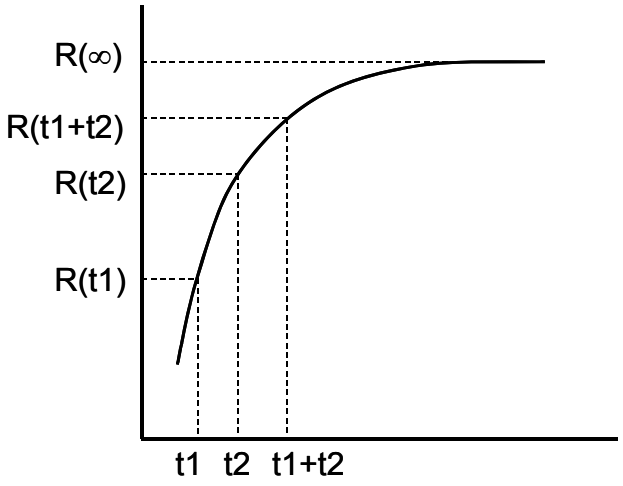


Fig. 6-9 Transient thermal resistance curve

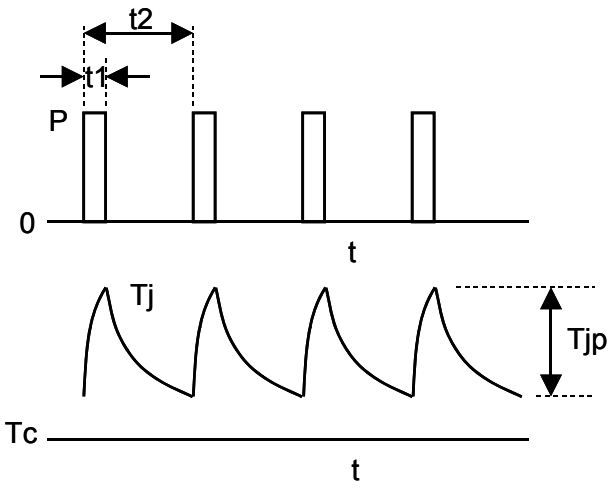


Fig. 6-10 Thermal ripples

3 Heat sink mounting precautions

3-1 Heat sink mounting

Since thermal impedance depends on IGBT mounting position, following attention should be taken into account:

- When mounting single IGBT module, the exact center of the heat sink generally results the lowest thermal impedance.
- When mounting multiple IGBT modules, determine the individual position on the heat sink according to the amount of heat generation from each module. Design more space for the modules that has higher heat generation.

3-2 Heat sink surface finishing

The mounting surface of the heat sink should be finished to a surface roughness of 10μm or less and a warpage of 50μm or less for every 100mm length. If the heat sink surface is not enough flat,
A drastic increase in the contact thermal resistance (Rth(c-f)) may be observed. If the flatness of the heat sink does not match the above requirements, IGBTs after mounted would have risk of extreme stress on the DBC substrate installed between the silicon chip and base plate. High voltage isolation failure would be concerned.

3-3 Thermal grease application

To obtain stable and low thermal contact resistance, a thermal greasing method between the heat sink and the IGBT base plate is highly recommended.

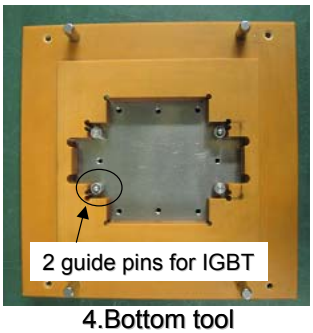
There are several methods of thermal grease application, such as roller, stencil mask and so on. Thermal grease helps the heat transfer from IGBT modules to heat sink, however the grease layer has also thermal capacity its. Therefore, when over thick thermal grease results chip temperature increase. On the other hand, extremely thermal grease application also may have a risk of chip temperature increase if the gap between the thermal grease and heat sink exists due to heat sink surface roughness or warpage. Therefore, the thermal grease layer must have the suitable thickness, otherwise the silicon chip may become higher than Tj(max), which results IGBT module destruction in the worst case. For these reasons, thermal grease application with stencil masks is recommended to help the uniform and stable application on the modules base plate.

Figure 6-11 shows the schematic view of the thermal grease application using a stencil mask. The basic procedure is to apply the specified weight of thermal grease to the base plate surface of the IGBT module through a stencil mask. Subsequently fix the thermal-greased IGBT modules are mounted on the heat sink by tightening the screws with specific mounting torque recommended for respective products. In this way, the thermal grease is applied uniformly. Fuji Electric can supply stencil mask patterns on request.

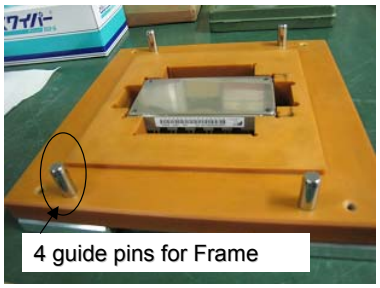
1.Back to Room Temp.

2.Mesure weight of IGBT

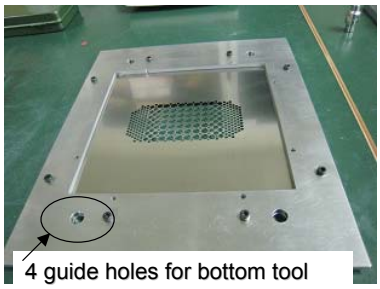
3.Adjust zero



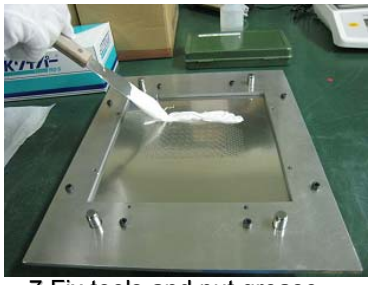
4.Bottom tool



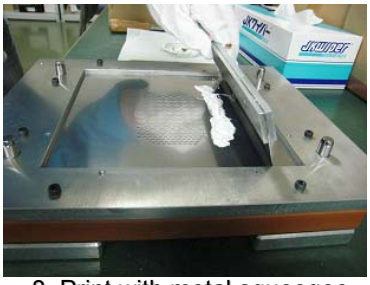
5.Set IGBT module



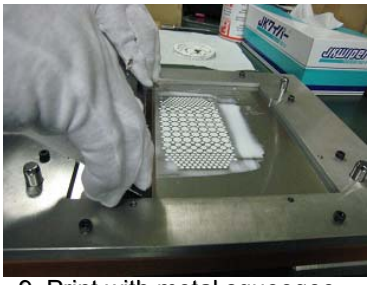
6.Metal mask and Frame



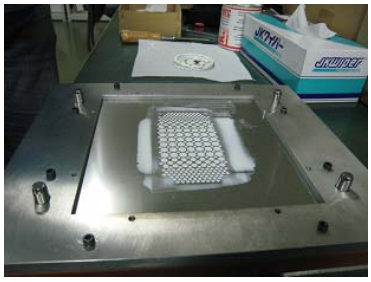
7.Fix tools and put grease with Knife



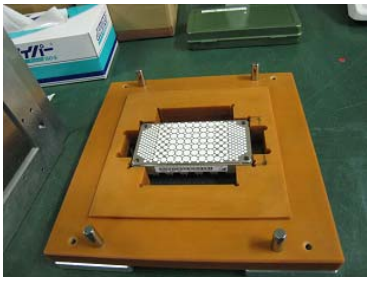
8. Print with metal squeegee (begin)



9. Print with metal squeegee (end)



10.After printing



11. Open metal mask

12. Check grease weight

Fig. 6-11 Schematic view of thermal grease application example

For the uniform thermal grease application, the required weight can be calculated as follows.

$$\text{Thermal grease thickness (um)} = \frac{\text{Weight of thermal grease (g)} \times 10^4}{\text{Baseplate area of IGBT module (cm}^2\text{)} \times \text{Density of thermal grease (g/cm}^3\text{)}}$$

It is recommended to estimate minimum weight of the thermal grease from the formula above before applying the the thermal grease. The recommended thickness thermal grease after mounted is 100μm.

However, the optimal thickness of thermal grease should be properly decided because it depends on the grease characteristics and its application method.

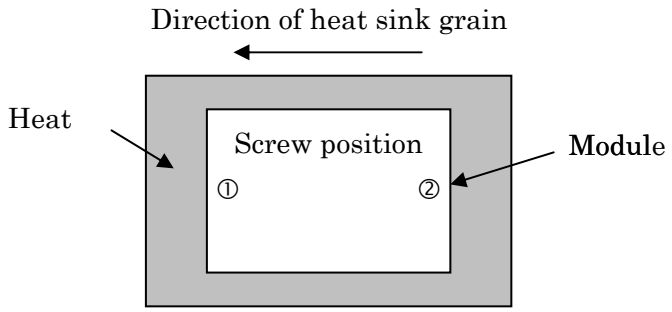
The recommended types of thermal grease are shown in Table 6-1.

Table 6-1 Example of thermal grease

Product name	Manufacturer
G746	Shin-Etsu Chemical Co., Ltd.
TG221	Nihon Data Material Co.,Ltd
SC102	Toray Dow-Corning Co., Ltd.
YG6260	Toshiba Silicone Co., Ltd.
P12	Wacker Chemie AG
HTC	ELECTROLUBE.

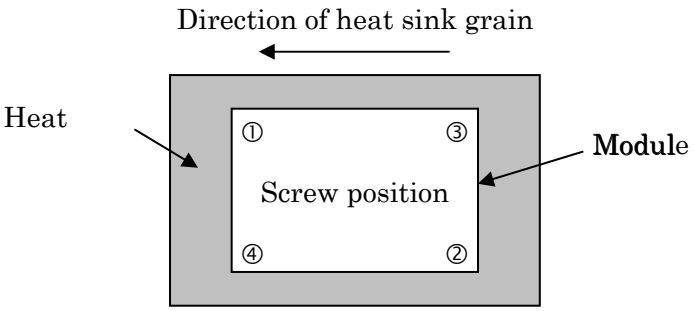
3-4 Mounting procedure

Diagrams in Figure 6-12 show how to tighten mounting screws to IGBT modules. Each screw must be tightened within a specified torque range, which is indicated in each IGBT module specification. An insufficient tightening torque may cause the poor contact thermal resistance and/or become mechanically loose during operation. On the other hand, an over torque may physically damage the IGBT case.



	Torque	Sequence
Initial	1/3 specified torque	①→②
Final	Full specified torque	②→①

(1) Two-points mounting



	Torque	Sequence
Initial	1/3 specified torque	①→②→③→④
Final	Full specified torque	④→③→②→①

(2) Four-points mounting

Fig. 6-12 Screw sequence for IGBT module

3-5 IGBT module mounting direction

When mounting the IGBT module on extrusion heatsink, it is recommended to place the module lengthwise in the direction of the heat sink grain. This reduces the effects of physical deformation of the heat sink shape.

3-6 Temperature verification

After deciding mounting position of IGBT module on the heatsink it is recommended to check the temperature of each position and confirm that the junction temperature (T_j) of each module if is within the design range.
For reference, Fig.6-12 is a diagram of how to measure the case temperature (T_c).

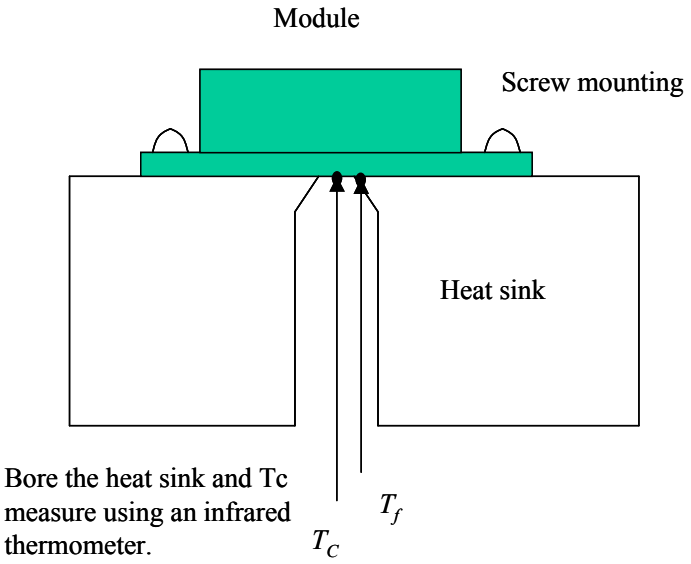


Fig. 6-13 Measurement of case temperature (Tc)

Chapter 7

Gate Drive circuit Design

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This section explains the drive circuit design.

In order to maximize the performance of an IGBT, it is important to properly set the drive circuit constants

1 IGBT drive conditions and main characteristics

IGBT drive conditions and main characteristics are shown below. An IGBT's main characteristics change according to the values of VGE and RG, so it is important to use settings appropriate for the intended use of the equipment in which it will be installed.

Table 7-1 IGBT drive conditions and main characteristics

Main characteristics	$+V_{GE}$ rise	$-V_{GE}$ rise	$R_{G(ON)}$ rise	$R_{G(oFF)}$ rise
$V_{CE(sat)}$	Fall	-	-	-
t_{on} E_{on}	Fall	-	Rise	-
t_{off} E_{off}	-	Fall	Rise	Rise
Turn-on surge voltage	Rise	-	Fall	-
Turn-off surge voltage	-	Rise	-	Fall *1
dv/dt malfunction	Rise	Fall	Fall	Fall
Current limit value	Rise	-	-	-
Short circuit withstand capability	Fall	-	-	-
Radiation EMI noise	Rise	-	Fall	Fall

*1: Dependence of surge voltage on gate resistance is different for each series

1.1 $+V_{GE}$ (On state)

A recommended the gate on state voltage value (+ V_{GE}) is +15V. Notes when + V_{GE} is designed are shown as follows.

(1) Set $+V_{GE}$ so that is remains under the maximum rated G-E voltage, V_{GES} =±20V.
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) The on-state C-E saturation voltage $V_{GE(sat)}$ is inversely dependent on $+V_{GE}$, so the greater the $+V_{GE}$ the smaller the $V_{GE(sat)}$.
(4) Turn-on switching time and switching loss grow smaller as $+V_{GE}$ rises.
(5) At turn-on (at FWD reverse recovery), the higher the $+V_{GE}$ the greater the likelihood of surge voltages in opposing arms.
(6) Even while the IGBT is in the off-state, there may be malfunctions caused by the dv/dt of the FWD's reverse recovery and a pulse collector current may cause unnecessary heat generation. This phenomenon is called a dv/dt shoot through and becomes more likely to occur as $+V_{GE}$ rises.
(7) In V and U series IGBTs, the higher the $+V_{GE}$, the higher the current limit becomes.
(8) The greater the $+V_{GE}$ the smaller the short circuit withstand capability.

1.2 $-V_{GE}$ (Off state)

A recommended the gate reverse bias voltage value ($-V_{GE}$) is –5 to -15V. Notes when $-V_{GE}$ is designed are shown as follows.

(1) Set $-V_{GE}$ so that it remains under the maximum rated G-E voltage, V_{GES} =±20V .
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) IGBT turn-off characteristics are heavily dependent on $-V_{GE}$, especially when the collector current is just beginning to switch off. Consequently, the greater the $-V_{GE}$ the shorter, the switching time and the switching loss become smaller.
(4) If the $-V_{GE}$ is too small, dv/dt shoot through currents may occur, so at least set it to a value greater than –5V. If the gate wiring is long, then it is especially important to pay attention to this.

1.3 R_G (Gate resistance)

Gate resistance R_G listed in the product specification sheets is the value on the condition so as to decrease the switching losses. So, you must select the optimal R_G according to the circuit or operating condition. Notes when R_G is designed are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G, and therefore the greater the R_G the longer the longer the switching time and the greater the switching loss. Also, as R_G increases, the surge voltage during switching becomes smaller.
(2) The greater the R_G the more unlikely a dv/dt shoot through current becomes.
(3) Various switching characteristics are varied for stray inductance. Especially, spike voltages when IGBTs are turned off or FWDs are recovered reversibly are influenced on the stray inductance. Therefore, RG need to be designed on the lower stray inductance condition.

Select the most suitable gate drive conditions while paying attention to the above points of interdependence.

1.4 avoid the unexpected turn-on by recovery dV/dt

In this section, the way to avoid the unexpected IGBT turn-on by dV/dt at the FWD's reverse recovery will be described.

Fig.7-1 shows the principle of unexpected turn-on caused by dV/dt at reverse recovery. In this figure, it is assumed that IGBT1 is turned off to on and gate to emitter voltage V_{GE} of IGBT2 is negative biased. In this condition, when IGBT1 get turned on from off-state, FWD on its opposite arm, that is, reverse recovery of FWD2 is occurred. At same time, voltage of IGBT2 and FWD2 with off-state is raised. This causes the dV/dt according to switching time of IGBT1.

Because IGBT1 and 2 have the mirror capacitance C_{GC}, Current is generated by dV/dt through C_{GC}. This current is expressed by C_{GC} x dV/dt. This current is flowed through the gate resistance R_G, results in increasing the gate potential. So, V_{GE} is generated between gate to emitter. If V_{GE} is excess the sum of reverse biased voltage and

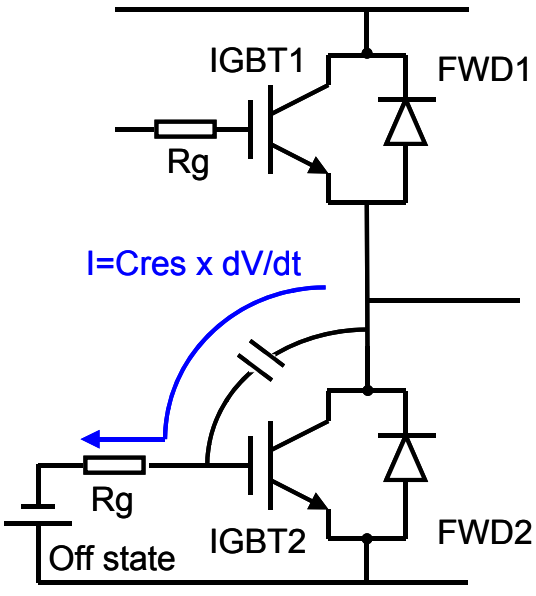
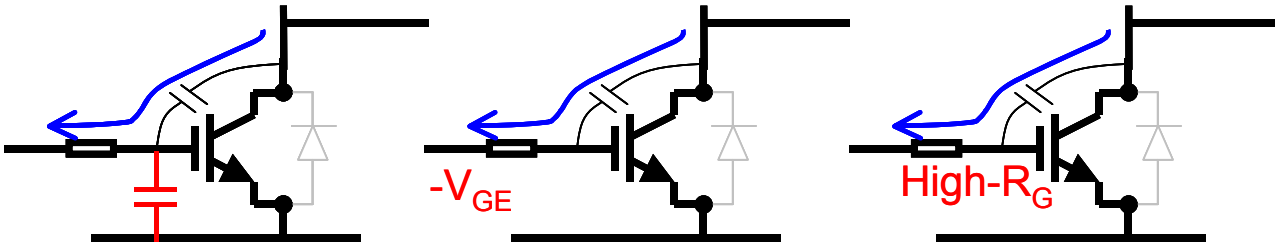


Fig.7-1 Principle of unexpected turn-on

V_{GE}(th), IGBT2 is turned on. Once IGBT2 is turned on, the short-circuit condition is happened, because both IGBT1 and 2 is under turned-on state.

From this principle, the methods to avoid the unexpected turn-on are shown in Fig.7-2. There are three methods, which are the C_{GE} addition, increase of reverse bias voltage and increase of R_G.



(a) additional Cge (b) increase of -Vge (c) increase of RG

Fig. 7-2 Methods to avoid unexpected turn-on

The method to add the C_{GE} is the way to the decrease of unexpected turn-on current by sharing to C_{GE}. Sharing current charges and/or discharges the additional CGE. In order to charge and/or discharge the additional CGE, switching speed gets lower. Just only adding the CGE results in the increase switching losses. However, lower Rg adding CGE at the same time can control switching speed. In other words, both adding the CGE and decreasing the RG can avoid the unexpected turn-on without increasing switching losses.

Driving higher R_G can decrease dV/dt, results in soft-switching. However, it has the disadvantage of increase switching losses as well. Moreover, although the method to enlarge the reverse bias is also effective to avoid the unexpected turn-on, the quantity of the gate charge becomes larger.

From these viewpoints, adding the C_{GE} is recommended to avoid unexpected turn-on. Recommended C_{GE} is two times value on the specification sheet and Recommended R_G is the half before adding C_{GE}. In this case, you must confirm the various characteristics.

2 Drive current

Since an IGBT has a MOS gate structure, to charge and discharge this gate when switching, it is necessary to make gate current (drive current) flow. Fig.7-3 shows the gate charge (dynamic input) characteristics. These gate charge dynamic input characteristics show the electric load necessary to drive the IGBT and are used to calculate values like average drive voltage and the driving electric power. Fig.7-4 shows the circuit schematic as well as the voltage and current waveforms. In principle, a drive circuit has a forward bias power supply alternately switching back and forth using switch S_1 and S_2. During this switching, the current used to charge and discharge the gate, is the driven current. In Fig. 7-4, the area showing the current waveform (the dotted area) is equivalent to the gate charge from Fig.7-3.

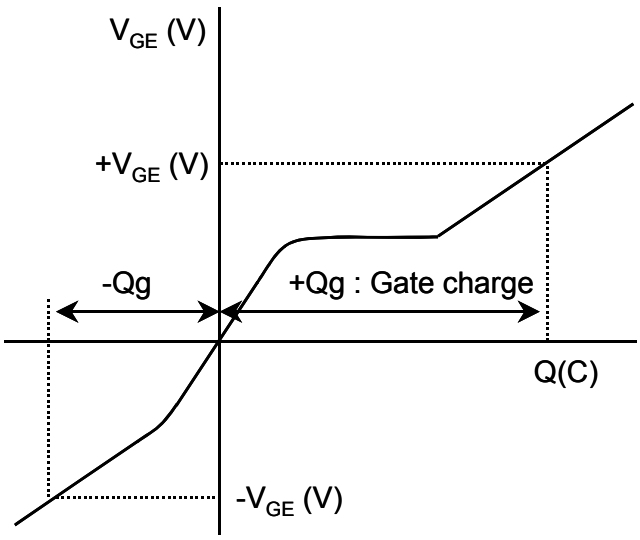


Fig. 7-3 Schematic waveform of gate charge characteristics (Dynamic input characteristics).

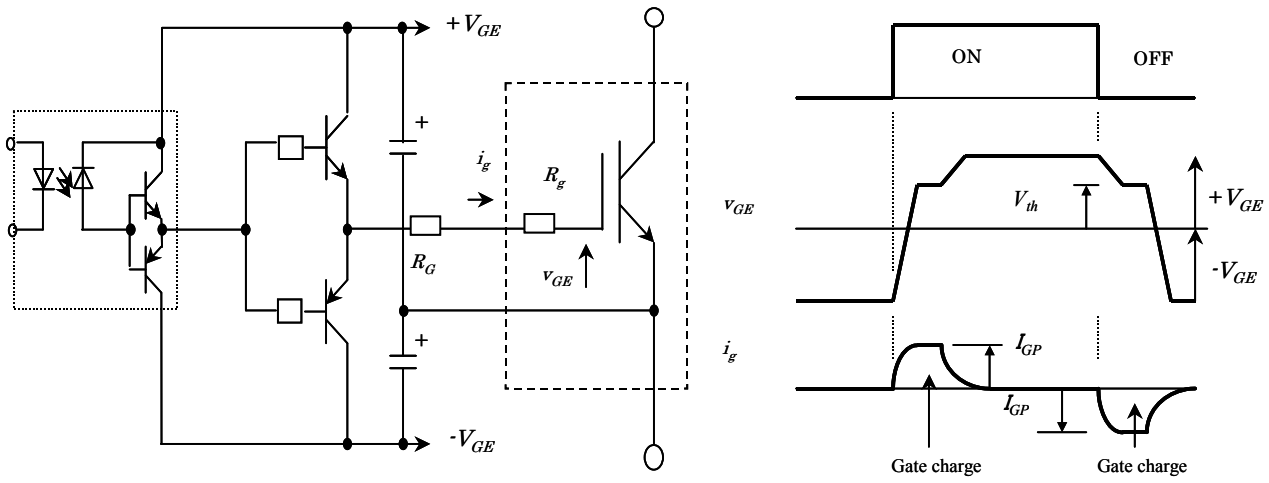


Fig. 7-4 Drive circuit schematic as well as voltage and current waveforms.

The drive current peak value I_{GP} can be approximately calculated as follows:

$$I_{GP} = \frac{+V_{GE} + |-V_{GE}|}{R_G + R_g}$$

$+V_{GE}$: Forward bias supply voltage
$-V_{GE}$: Reverse bias supply voltage
R_G : Drive circuit gate resistance
R_g : Module's internal resistance

Internal gate resistance Rg is various for each type name or series. Therefore, refer to application manual for application manual or technical data.

On the there hand, the average value of the drive current I_G, using the gate charge characteristics (Fig.7-3), can be calculated as follows:

$$+I_G = -I_G = fc \times \left(|+Q_g| + |-Q_g|\right)$$

fc : Carrier frequency
Q_g : Gate charge from 0V to $+V_{GE}$
$-Q_g$: Gate charge from $-V_{GE}$ to 0V

Consequently, it is important to set the output stage of the drive circuit in order to conduct this approximate current flow (I_{GP}, as well as $\pm I_G$).

Furthermore, if the power dissipation loss of the drive circuit is completely consumed by the gate resistance, then the drive power (Pd) necessary to drive the IGBT is shown in the following formula:

$$Pd(on) = fc \bullet \left[\frac{1}{2}\left(|+Q_g| + |-Q_g|\right) \bullet \left(|+V_{GE}| + |-V_{GE}|\right)\right]$$

$$Pd(off) = Pd(on)$$

$$Pd = Pd(off) + Pd(on)$$

$$= fc \bullet \left(|+Q_g| + |-Q_g|\right) \bullet \left(|+V_{GE}| + |-V_{GE}|\right)$$

Accordingly, a gate resistance is necessary that can charge this approximate capacity.

Be sure to design the drive circuit so that the above-mentioned drive current and drive power can be properly supplied.

3 Setting dead-time

For inverter circuits and the like, it is necessary to set an on-off timing “delay” (dead time) in order to prevent short circuits. During the dead time, both the upper and lower arms are in the “off” state. Basically, the dead time (see Fig.7-5) needs to be set longer than the IGBT switching time (toff max.).

For example, if RG is increased, switching time also becomes longer, so it would be necessary to lengthen dead time as well. Also, it is necessary to consider other drive conditions and the temperature characteristics.

It is important to be careful with dead times that are too short, because in the event of a short circuit in the upper or lower arms, the heat generated by the short circuit current may destroy the module.

Therefore, the dead time of more than 3usec would be recommended for IGBT modules. However, appropriate dead time should be settled by the confirmation of practical machine.

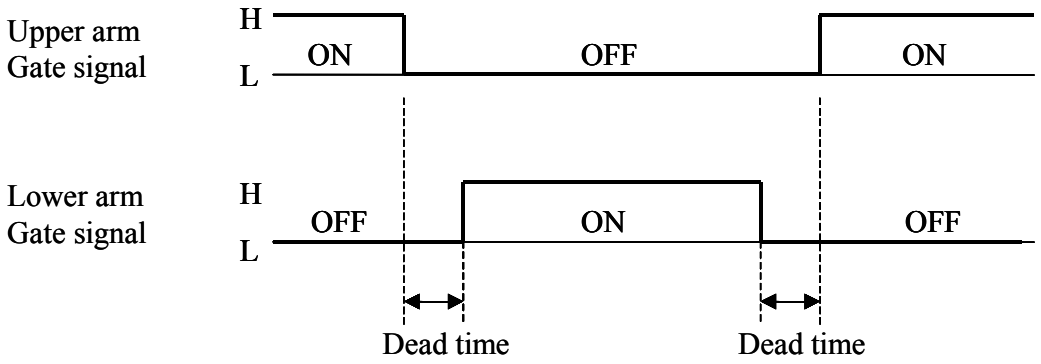
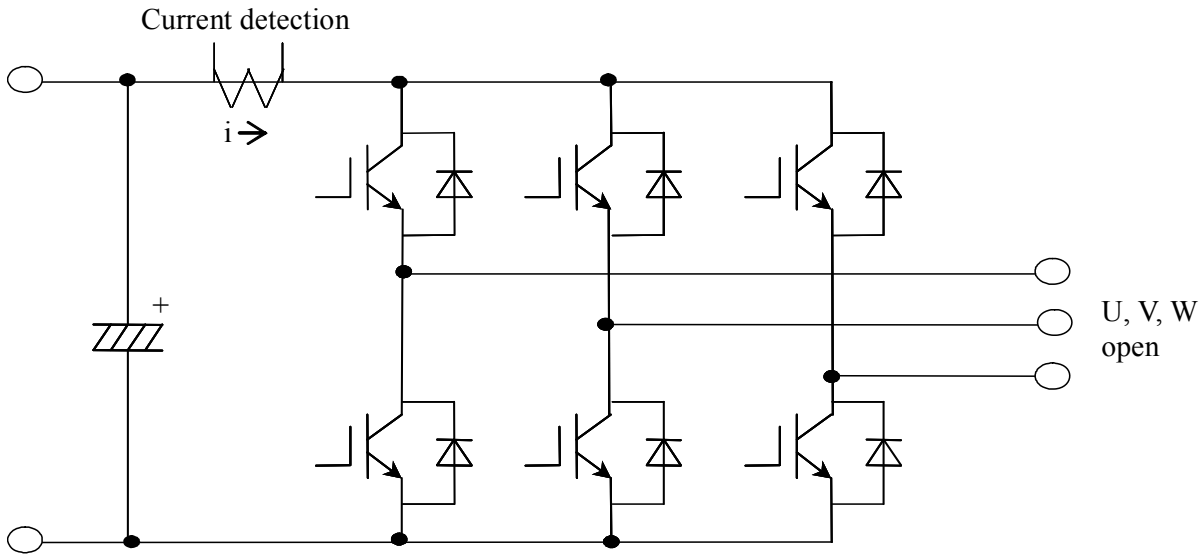


Fig. 7-5 Dead time timing chart.

One method of judging whether or not the dead time setting is sufficient or not, is to check the current of a no-load DC supply line.

In the case of a 3-phase inverter (as shown in Fig.7-4), set the inverter's outputs to open, then apply a normal input signal, and finally measures the DC line current. A very small pulse current (dV/dt current leaving out the module's Miller Capacitance: about 5% of the normal rated current) will be observed, even if the dead time is long enough.

However, if the dead time is insufficient, then there will be a short circuit current flow much larger than this. In this case, keep increasing the dead time until the short circuit current disappears. Also, for the same reasons stated above, we recommend testing at high temperatures.



Insufficient dead time makes short circuit current much larger than dv/dt current.

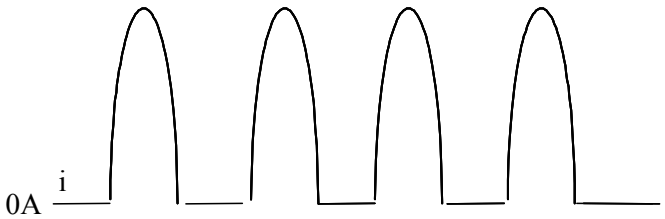


Fig. 7-6 Current detection methods for short circuit cased by insufficient dead time.

4 Concrete examples of drive circuits

For inverter circuits and the like, it is necessary to electrically isolate the IGBT from the control circuit. An example of a drive circuit using this principle, is shown below.

Fig.7-7 shows an example of a drive circuit using a high speed opto-coupler. By using the opto-coupler, the input signal and the module are isolated from each other. Also, since the opto-coupler does not limit the output pulse width, it is suitable for changing pulse widths or PWM controllers, to wide ranges. It is currently the most widely used.

Furthermore, this way the turn-on and turn-off characteristics determined by gate resistance can be set separately, so it commonly used to ensure the best settings.

Aside from the above, there is also a signal isolation method using a pulse transformer. With this method the signal as well as the gate drive power can both be supplied simultaneously from the signal side, thereby allowing circuit simplification. However, this method has the limitations of an on/(off+on) time ratio of max. 50%, and reverse bias cannot be set, so its usefulness as a control method and switching frequency regulator is limited.

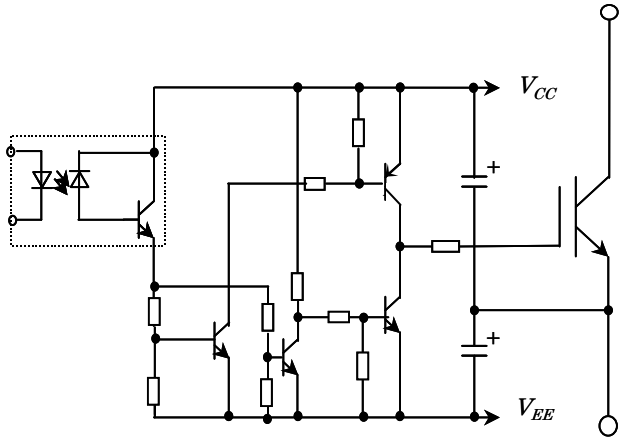


Fig. 7-7 Example of drive circuit using high speed opto-coupler.

5 Drive circuit setting and actual implementation

5.1 Opto-coupler noise ruggedness

As IGBTs are high speed switching elements, it is necessary to select a opto-coupler for drive circuit that has a high noise ruggedness (e.g. HCPL4504). Also, to prevent malfunctions, make sure that the wiring from different sides doesn't cross. Furthermore, in order to make full use of the IGBT's a high speed switching capabilities, we recommend using a opto-coupler with a short signal transmission delay.

5.2 Wiring between drive circuit and IGBT

If the wiring between the drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. A countermeasure for this is shown below in Fig.7-8.

(1) Make the drive circuit wiring as short as possible and finely twist the gate and emitter wiring. (Twist wiring)
(2) Increase RG. However, pay attention to switching time and switching loss.
(3) Separate the gate wiring and IGBT control circuit wiring as much as possible, and set the layout so that they cross each other (in order to avoid mutual induction).
(4) Do not bundle together the gate wiring or other phases.

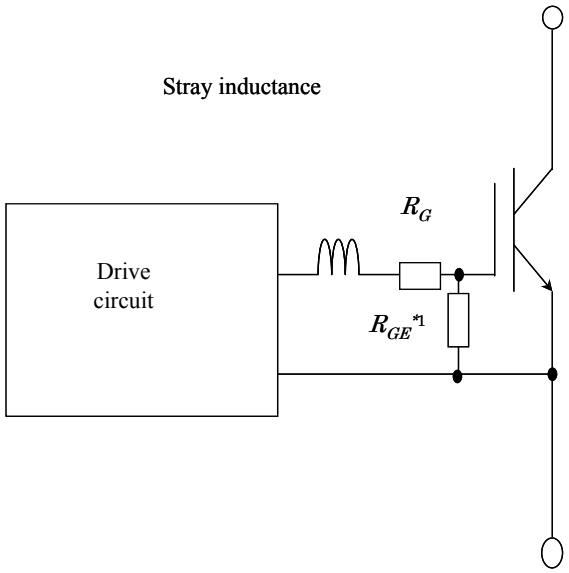


Fig. 7-8 Gate signal oscillation countermeasure

*1 R_{GE}

If the gate circuit is bad or if the gate circuit is not operating (gate in open state)*2 and a voltage is applied to the power circuit, the IGBT may be destroyed. In order to prevent this destruction, we recommend placing a 10kΩ resistance R_{GE} between the gate and emitter.

*2 Switch-on

When powering up, first switch on the gate circuit power supply and then when it is fully operational, switch on the main circuit power supply.

5.3 Gate overvoltage protection

It is necessary that IGBT modules, like other MOS based elements, are sufficiently protected against static electricity. Also, since the G-E absolute maximum rated voltage is ±20V, if there is a possibility that a voltage greater than this may be applied, then as a protective measure it is necessary to connect a zener diode between the gate and emitter as shown in Fig.7-9.

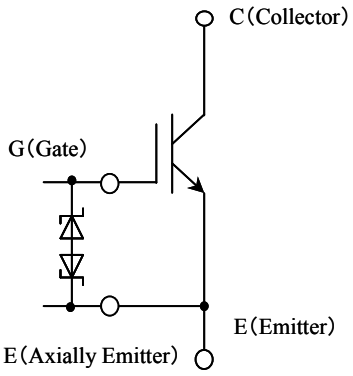


Fig. 7-9 G-E overvoltage protection circuit example.

Chapter 8

Parallel Connections

CONTENTS

This chapter explains the notes when IGBT is connected in parallel.

IGBTs would be connected in parallel in order to enlarge the current capability. In this case, the number of parallel-connected modules has no limitation. However you have to consider some disadvantages of noise or spike voltage increase, which are caused by longer interconnections.

You have to pay attention to the following basic notes when connecting IGBT modules in parallel.

1. Suppression of current imbalance at steady states
2. Suppression of current imbalance at dynamic state of turn-on or turn-on
3. Symmetry of gate drive circuit

1 On-state current imbalance

An on-state current imbalance may be mainly caused by the following two factors:
(1) $V_{CE(sat)}$ distribution
(2) Main circuit wiring resistance distribution

1.1 Current imbalance caused by VCE(sat) distribution

As shown in Fig.8-1, a difference in the output characteristics of two IGBT modules connected in parallel can cause a current imbalance.

The output characteristics of Q_1 and Q_2 shown in Fig.8-1, can be approximated as follows:

$$V_{CEQ1} = V_{01} + r_1 \times I_{C1}$$

$$r_1 = V_1 / (I_{C1} - I_{C2})$$

$$V_{CEQ2} = V_{02} + r_2 \times I_{C2}$$

$$r_2 = V_2 / (I_{C1} - I_{C2})$$

Based on the above, if the I_{Ctotal} ($=I_{C1}+I_{C2}$) collector current is made to flow through the circuit of Q_1 and Q_2 connected in parallel, then the IGBT's collector current becomes the following:

$$I_{C1} = (V_{02} - V_{01} + r_2 \times I_{Ctotal}) / (r_1 + r_2)$$
$$I_{C2} = (V_{01} - V_{02} + r_1 \times I_{Ctotal}) / (r_1 + r_2)$$

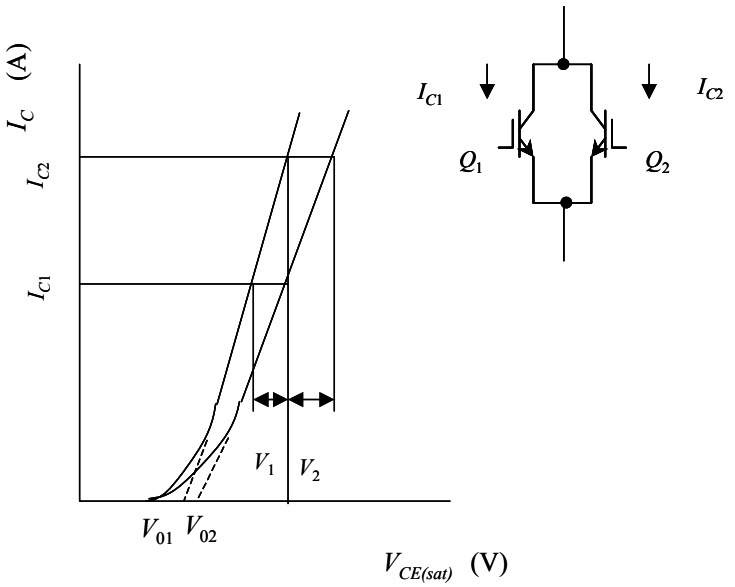


Fig. 8-1 Example of a $V_{CE(sat)}$ pair

For simplicity, assuming $V_{01}=V_{02}$ in the above equations, I_{C1} could be r_2/r_1 times larger than I_{C2}. This result means that current sharing for Q1is larger than Q2.

In this way, $V_{CE(sat)}$ becomes a major factor in causing current imbalances. Therefore, in order to ensure the desired current sharing it is necessary to pair modules that have a similar $V_{CE(sat)}$ which is small variation. $V_{CE(sat)}$ distribution can be minimized with the use of the same production lot, because influence of fabrication processes is minimized. From this reason, connecting IGBT modules in parallel is recommended with the use of the same production lot.

1.2 Current imbalance by main circuit wiring resistance distribution

The equivalent circuit with the main circuit's wiring resistance is shown in Fig. 8-2. The effect is larger with emitter resistance than with collector resistance, so collector resistance has been omitted here. If there is resistance in the main circuit as shown in Fig.8-2, then the slope of the IGBT modules' output characteristics will lessen, and the collector current will drop in comparison without emitter resistance. In addition, if $R_{E1}>R_{E2}$, then the slope of the Q_1 output characteristics will lessen and if $I_{C1}<I_{C2}$ then a current sharing imbalance will appear. Moreover, if gate voltage is applied without extra-emitter terminals for parallel-connected IGBTs, the actual gate-emitter voltage drop (V_{GE}=V – VE) will be decreased, because an electrical potential difference may appear, depending on how well the collector current can flow through this resistance. So, the IGBTs' output characteristics change and the collector current decline.

Therefore, in order to reduce this imbalance, it is necessary to make the wiring on the emitter side as short and as uniform as possible as well as to apply the gate voltage between gate terminal and additional emitter terminal.

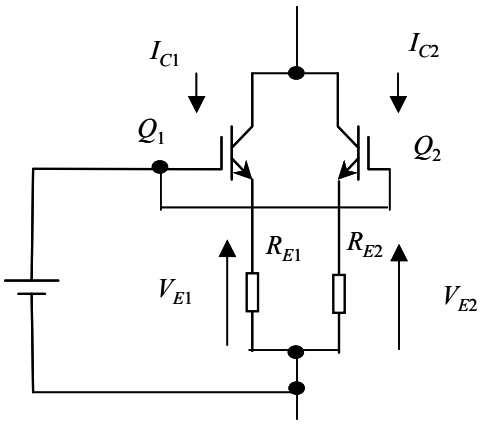


Fig. 8-2 The effect of main circuit wiring resistance

1.3 Tj dependence of output characteristics and current imbalance

Tj dependency of output characteristics deeply affects current imbalance. Here, output characteristic, whose VCE(sat) is higher and lower with the increase of Tj, is respectively defined as the positive and negative Tj dependency. Fig. 8-3 shows the representative output waveform with negative and positive dependency, which are 100A rating. Collector current at the same Vce is decreased as Tj is increased in case of positive dependency.

As described 1-1, shared current of IGBT with lower VCE(sat) is larger at the parallel connecting. Therefore, steady-state loss is larger for IGBT with lower VCE(sat) than another to increase junction temperature. In this way, in case of positive dependency of IGBT, this leads to make shared current between them balanced. On the contrary, in case of negative dependency, current sharing is act as opposite work. Therefore, you need to pay attention to current imbalance in designing the machines or components. Selecting the IGBTs with the positive dependency of output characteristic is recommended when IGBTs are parallel-connected, because IGBTs with positive dependency of output characteristic are relatively easier to use for parallel connection of IGBTs than that with negative one. Further, for IGBT series after 4th generation S-series, Tj dependency of output characteristic is positive.

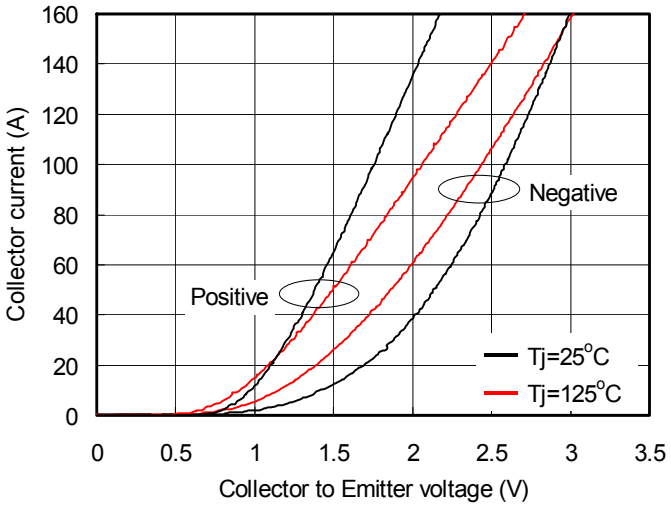


Fig. 8-3 Comparison output characteristics

Please refer to the each series specification for details of Tj dependency of output characteristic.

1.4 Deviation of VCE(sat) and current imbalance rate

Ratio of shared current in parallel connection is called as current imbalance rate, which is determined by deviation of VCE(sat) and Tj dependency of put characteristic.

Fig. 8-4 shows the representative relationship between deviation of VCE(sat) and current imbalance rate. This figure is an example for 2 parallel connections of V-series IGBTs. From this figure, current imbalance rate is found to be larger as deviation of $V_{CE(sat)}$ is increased. Therefore, it is important to use IGBTs for parallel connection, whose deviation of VCE(sat) is small, that is, ΔVCE(sat) is small.

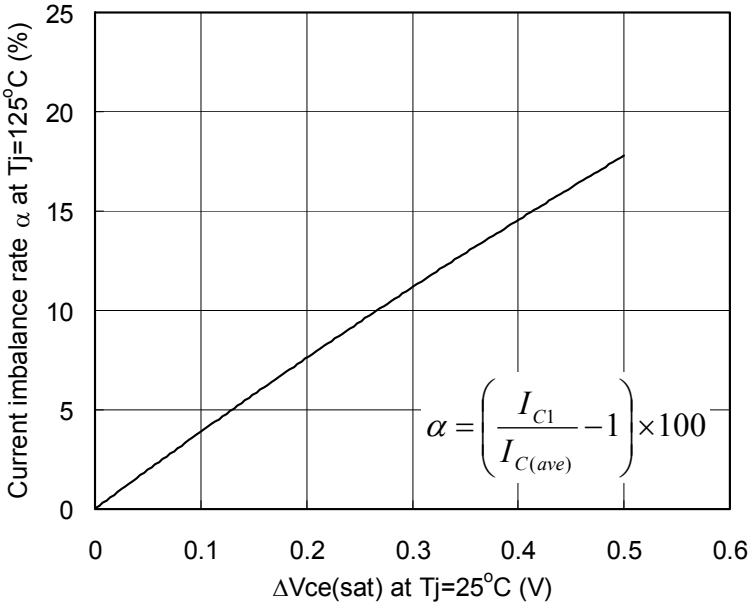


Fig. 8-4 Deviation of $V_{CE(sat)}$ and current imbalance rate

1.5 Derating in parallel connection using many numbers of IGBTs

Derating (Decrease of total current) is needed in consideration with current imbalance in parallel connection of IGBTs.

When n-number of modules are connected in parallel, the following shows the maximum current that can be applied under the worst case conditions where the entire current is concentrated into one module, whose VCE(sat) is the smallest. Therefore, available maximum current □I is expressed by □, which is connected in parallel using 2 modules:

$$\sum I = I_{C(\max)} \left[1 + (n-1) \frac{\left(1 - \frac{\alpha}{100}\right)}{\left(1 + \frac{\alpha}{100}\right)} \right] \qquad \alpha = \left(\frac{I_{C1}}{I_{C(ave)}} - 1 \right) \times 100$$

Here $I_{C(max)}$ represents the maximum current for a single element, □I represents the maximum current in parallel connection. However, to operate in total current □I, each module connected in parallel is satisfied with the RBSOA on the specification, Tj(max) for dissipation wattage as well. Note especially that Tj rise caused by dissipation wattage is various on the condition such as switching frequency, driving condition, cooling condition and snubber condition and so on.

For example, if α=15%, $I_{C(max)}$=200A and n=4, then ΣI=643.4A, and the parallel connected total current should be set so as not to exceed this value. In this case, Derating of 19.6% is needed. In this way, the parallel connected total current is need to be derated for simply calculating n x $I_{C(max)}$.

Fig. 8-5 shows the derating rate for □=15%. It is found from this figurer that derating rate is increased as the parallel number n is larger. Therefore, derate the total current for parallel connection, depending on the parallel number n. in addition, note that derating rate is various by current imbalance rate.

Because derating rate for this example is a calculated value. It should be determined after confirmation and verification of imbalance current using designed machines.

If you need to change paralleled modules for troubles and/or maintenances, it is recommended that all the paralleled modules be exchanged. In this case, it is recommended that parallel connection be set up using IGBTs with the same production lots.

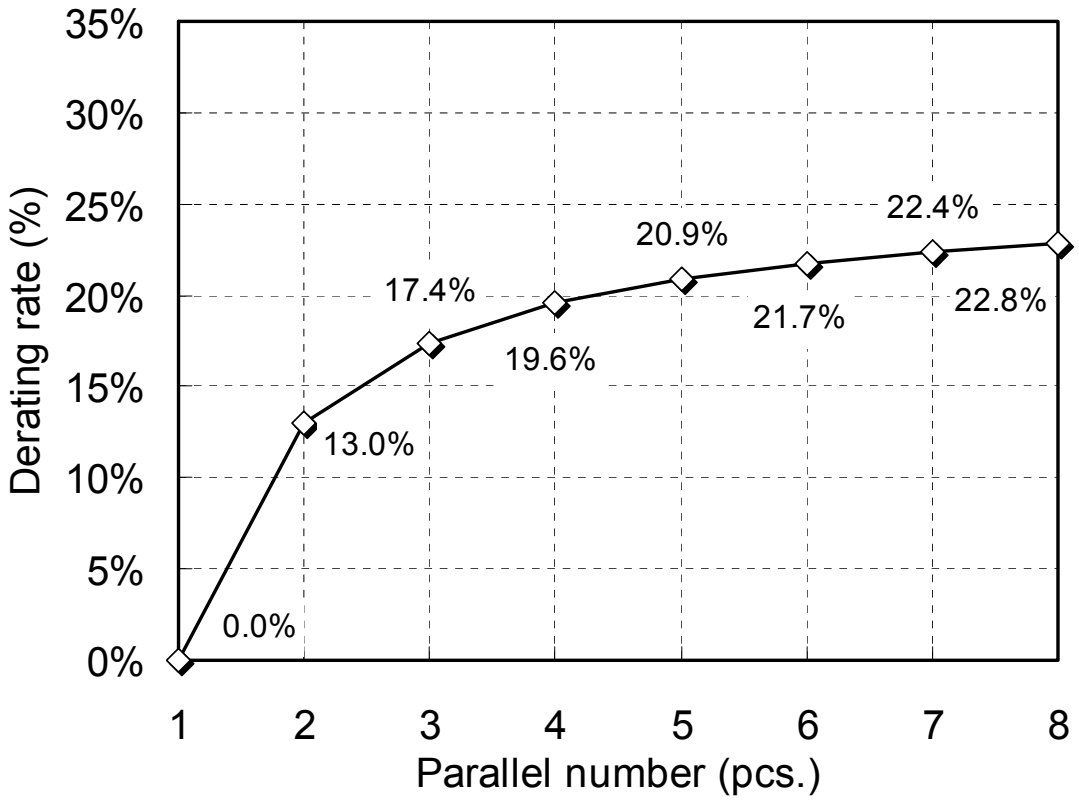


Fig. 8-5 Relationship between derating rate and parallel number

2 Current imbalance at switching

Current imbalance at switching may be mainly caused by the following two factors:

(1) Module characteristics distribution

(2) Main circuit wiring resistance distribution

2.1 Module characteristics distribution

An IGBTs' switching current imbalance, especially just before turn-off and after turn-on, is mostly determined by an on-state current imbalance, therefore if the on-state current imbalance is controlled simultaneously as shown previously, so will the switching voltage imbalance.

2.2 Main circuit wiring inductance distribution

Inhomogeneous main circuit wiring inductance caused current sharing. Fig. 8-6 shows the equivalent circuit at parallel connection in consideration with main circuit wiring inductance. When IC1 and IC2 flow through IGBT1 and 2 respectively, shared currents for them are approximately decided by the ratio of main circuit wiring inductance, LC1+LE1 and LC2+LE2. So, main circuit wiring is need to be connected as equally as possible in order to relieve current imbalance at switching. However, even if ideal wiring inductance of LC1+LE1=LC2+LE2 is realized, the difference between LE1 and LE2 causes the current imbalance as described bellows.

Inhomogeneous inductance between LE1 and LE2 causes the different inductive voltage originated di/dt at turn-on. This difference between their inductive voltages affects current imbalance more, because it biases to different way to gate to emitter voltage.

If the inductance of the main circuit is large, then the spike voltage at IGBT turn-off will also be high. Therefore, for the purpose of reducing wiring induction, consider setting the modules that are to be connected in parallel as close together as possible and making the wiring as uniform as possible.

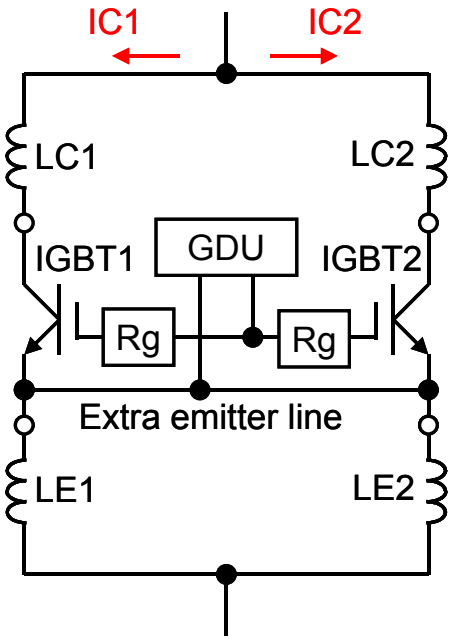


Fig. 8-6 Equivalent circuit at parallel connection in consideration with main circuit wiring inductance

3 Gate drive circuit

It would be worried that duration until switching (turn-off or turn-on) is varied by the delay time of gate driving unit (GDU), when each gate of parallel-connected modules is driven by each GDU, separately independent on the number of modules. Therefore, it is recommended that all the gates are driven by just only a GDU, when connecting modules in parallel. This can lead the decrease of deviation for different duration until switching.

At the same time, connect gate resistances between gate terminal of each module and a GDU so as to avoid the gate voltage oscillation caused by coupling gate wiring inductance with input capacitance of IGBT as shown in Fig.8-7.

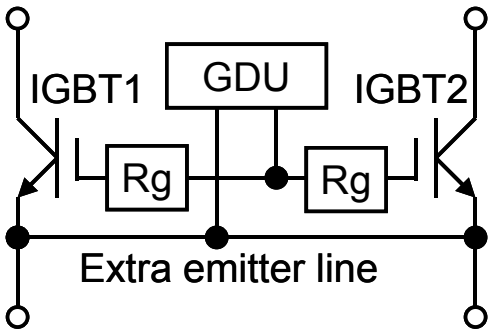


Fig.8-7 wiring gate drive unit

As stated previously, if the drive circuit's emitter wiring is connected in a different position from the main circuit, then the modules' transient current sharing (especially at turn-on) will become imbalanced, because LE1 is different from LE2 as described in Fig.8-6.

In general, IGBT modules have an auxiliary emitter terminal for use by drive circuits. By using this terminal, the drive wiring of each module becomes uniform, and transient current imbalances attribute to drive circuit wiring can be controlled. Furthermore, be sure to wind the drive circuit wiring tightly together, and lay it out so that it is as far away from the main circuit as possible in order to avoid mutual induction.

4 Wiring example for parallel connections

As described before, pay attention in order to connect the modules in parallel. Fig.8-7 shows the equivalent circuit with parallel-connected 2in1 modules. From this figure, it is found that all the wiring to parallel-connected IGBTs (IGBT1 and IGBT2) are connected symmetrically. This can realize the better current sharing.

Fig.8-9 shows the switching waveform with the two IGBT modules connected in parallel. IGBT modules of 1000A/1700V were applied. It is found from this figure that almost uniform current flows are realized, and current imbalance rate is only 2%.

Symmetrical wiring can help the much better current sharing.

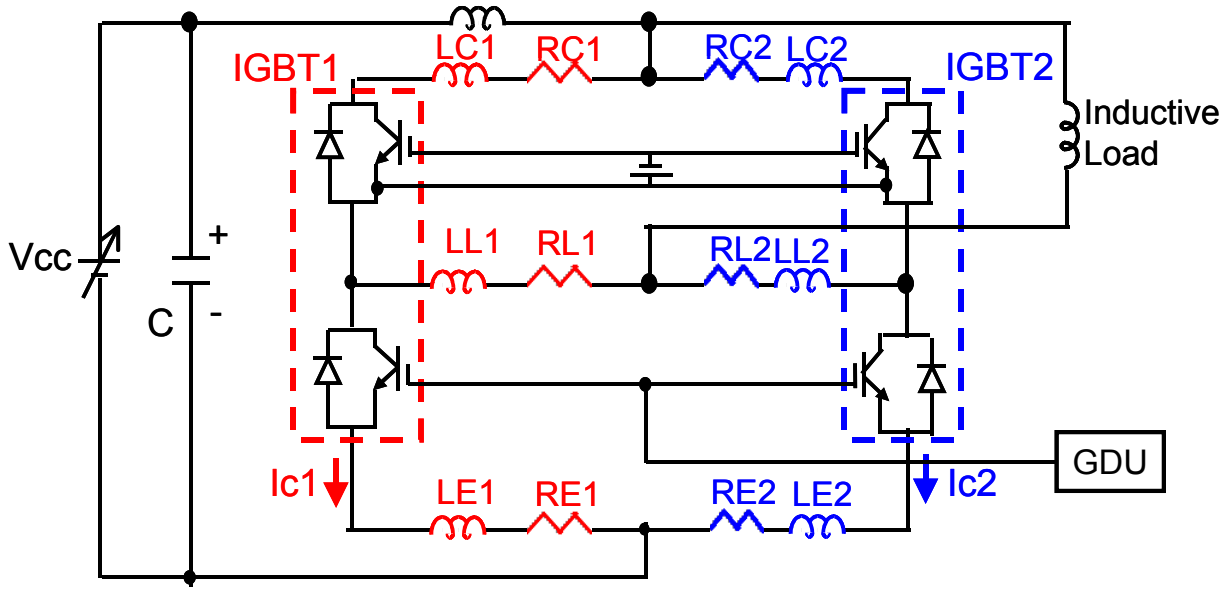


Fig. 8-7 Equivalent circuit with parallel-connected 2in1 modules

(Make the wiring RC1=RC2, RL1=RL2, RE1=RE2 LC1=LC2, LL1=LL2, LE1=LE2)

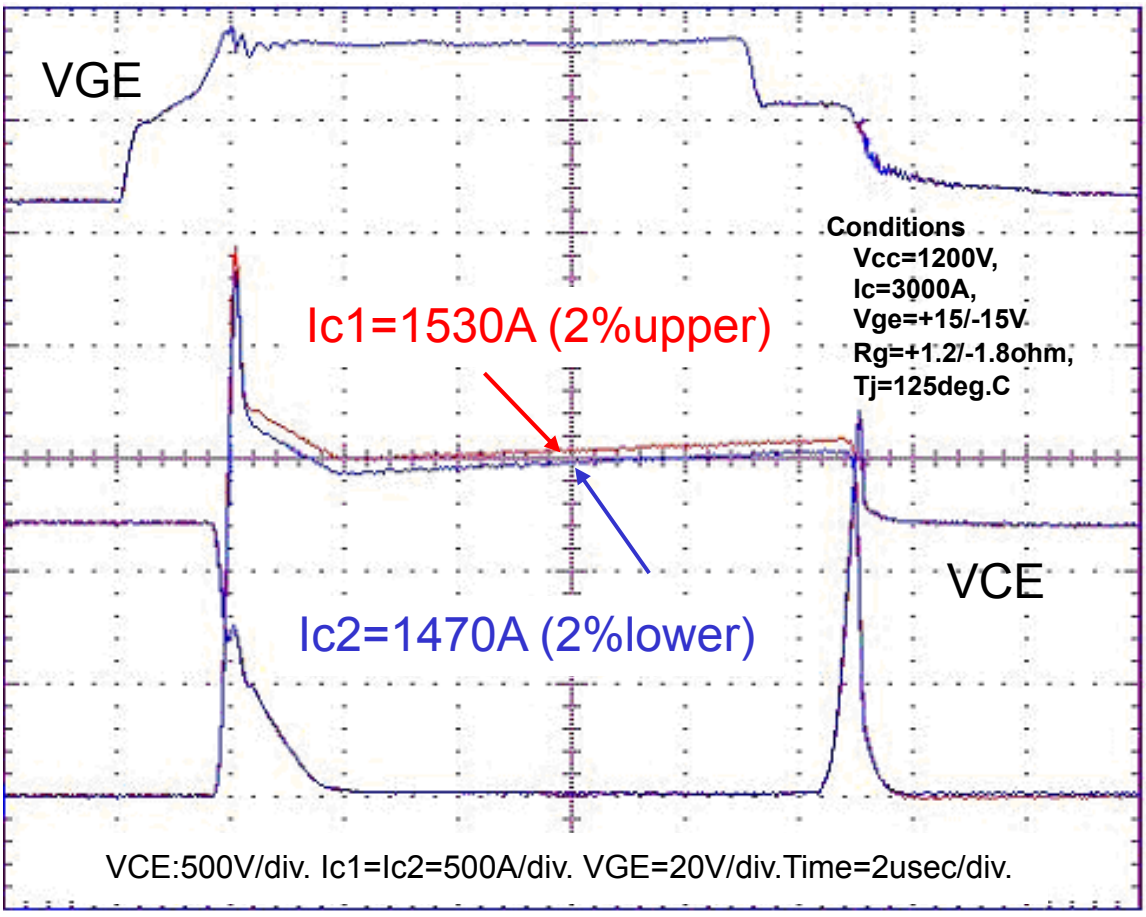


Fig. 8-8 Switching waveform with the two IGBT modules connected in parallel

(1000A/1700V 2in1 module : 2MBI1000VXB-170-50)

Chapter 9

Evaluation and Measurement

CONTENTS

This section explains the method of evaluating the IGBT module characteristics and the measurement methods.

1 Application scope

This chapter provides instructions on how to evaluate the characteristics of IGBT modules used in power electronics having a switching frequency of several kHz to 100 kHz and an equipment capacitance of several hundred VA or more. It also provides instructions on how to measure IGBT module voltage and current.

2 Evaluation and measurement methods

2.1 Evaluation and measurement method summary

While power electronic test equipment is always under development, and it is necessary to evaluate the characteristics of a semiconductor device and measure its performance during its installation into circuits, use the correct equipment to capture this information.

Table 9-1 gives a summary description of the evaluation items and measurement methods.

Table 9-1 Evaluation item and measurement method summary.

No.	Evaluation item	Measured quantity	Measurement methods	Measuring equipment
1	Isolation voltage	Voltage	With the module terminals shorted, apply a voltage between the conductive part and the frame of the device.	Isolation voltage tester
2	Collector– Emitter voltage		With the Gate and Emitter shorted, apply test voltage to the Collector and Emitter. *If the applied test voltage exceeds the V rating of components connected to C & E, disconnect those components.	Curve tracer
3	Collector-Emitter saturation voltage		Perform measurements with a voltage clamping circuit inserted between the Collector and Emitter to bypass the effect of the amplifier built in the oscilloscope. *Static characteristics can be measured with a curve tracer or pulse h_{FE} meter.	Oscilloscope
4	Spike voltage		Measure the voltage between the modules terminals directly for both the Collector and Emitter.	Oscilloscope
5	Switching time	Voltage Current	Measure the required voltage and current waveform according to the switching time definition.	Oscilloscope Current probe
6	Current sharing at parallel connection	Current	Measure the current through each device using current transformers for measurement.	Oscilloscope Current probe
7	Switching loss	Voltage Current	The product of the current and voltage is integrated during the switching time. (1) Calculate from the voltage and current waveforms. (2) Use a measuring instrument having math computing capability.	Oscilloscope
8	Operating locus		Plot the current and the voltage during switching action in current-voltage graph.	Oscilloscope with an X-Y display facility
9	Case temperature	Temperature	Measure on the copper base under the IGBT chip. *The case temperature measurement location is shown in chapter 3.	Thermocouple thermometer
10	Junction temperature		Have a calibration curve for the junction temperature and device characteristics created with regard to the temperature dependence of the device characteristics (for example, on resistance) and then measure the characteristics of the device in operation to estimate the junction temperature. *The method of measuring the junction temperature using the IR camera directly.	IR camera

2.2 Voltage measurement

Voltage measurement relates to the measurement of such voltages as the transient voltage during switching action, the voltage in the brief on-state following switching action etc. Note that the accuracy of voltage measurement is affected by the noise interferences imparted from large-amplitude fast switching action.

(1) Measuring apparatus and calibration

Voltages are usually measured using an oscilloscope for the measuring apparatus, because their waveform, as well as the measurement value, is important. Voltage probes are used for voltage measurement.

The time constants of the voltage divider RC of the probe and oscilloscope vary depending on the oscilloscope-probe combination. Before using the probe, carry out probe compensation to achieve uniform attenuation across the frequency range by using the calibrator output and voltage of the oscilloscope.

With an appropriate sensitivity setting (generally, 3 to 4 div amplitude on the display screen), set the input coupling to DC. Exercise caution in selecting the probe, because the adjustment capacitance of the probe and the input capacitance of the oscilloscope must match to enable adjustment.

The selection of oscilloscopes and probes are shown in sections 9-5 and 9-6.

(2) Saturation voltage measurement

Generally, while the circuit voltage under which an IGBT is used comes as high as several hundred Volts, the saturation voltage is as low as several Volts. Because the size of the screen used in an oscilloscope is generally finite, raising the voltage sensitivity in an effort to read the saturation voltage accurately will result in the display of a waveform that is different from the actual waveform, primarily because of the effect of the saturation of the oscilloscope's internal amplifier.

Accordingly, the IGBT saturation voltage during the switching action cannot be known by directly measuring the voltage between the device collector and emitter. Therefore, measure the saturation voltage by adding a voltage clamping circuit shown in Fig.9-1.

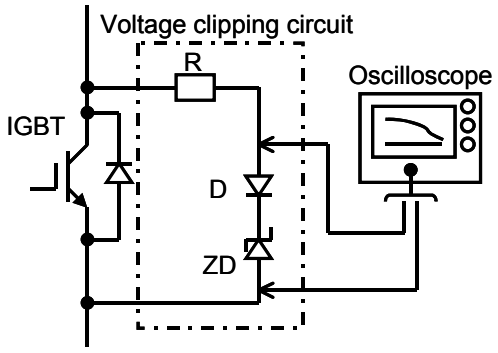


Fig.9-1 Saturation voltage measurement method

In Fig.9-1, the Zener diode (ZD) limits the high voltage when the IGBT is turned-off. Generally, a Zener diode of 10V or less is used. R denotes a current-limiting resistance. Because a large proportion of the circuit voltage is applied to this resistance when the IGBT is turned-off, the resistance must have a relatively large value. The diode (D) prevents the charges built in the junction capacitance of the Zener diode (ZD) from discharging, and also prevents a filter from being formed of the junction capacitance and the current-limiting resistance.

(3) Spike voltage measurement (Collector – emitter voltage measurement)

While IGBTs offer the benefit of fast switching, they have a high ratio of turn-off current change (-di/dt), inducing a high voltage in the main circuit wiring inductance (ls) of the equipment. This voltage is superimposed over the DC circuit voltage to creating a spike voltage to the module. It is necessary to verify that this voltage has a predefined voltage margin, established by the designer, with respect to the maximum voltage ratings.

The spike voltage can be measured at the terminals of the module with an oscilloscope and then directly reading the value on the screen. When making these measurements, keep the following precautions in mind:

(I) Use a probe and an oscilloscope having a sufficient frequency bandwidth.
(II) Adjust the oscilloscope sensitivity and calibrate the probe.
(III) Connect the measurement probe directly to the module terminals.

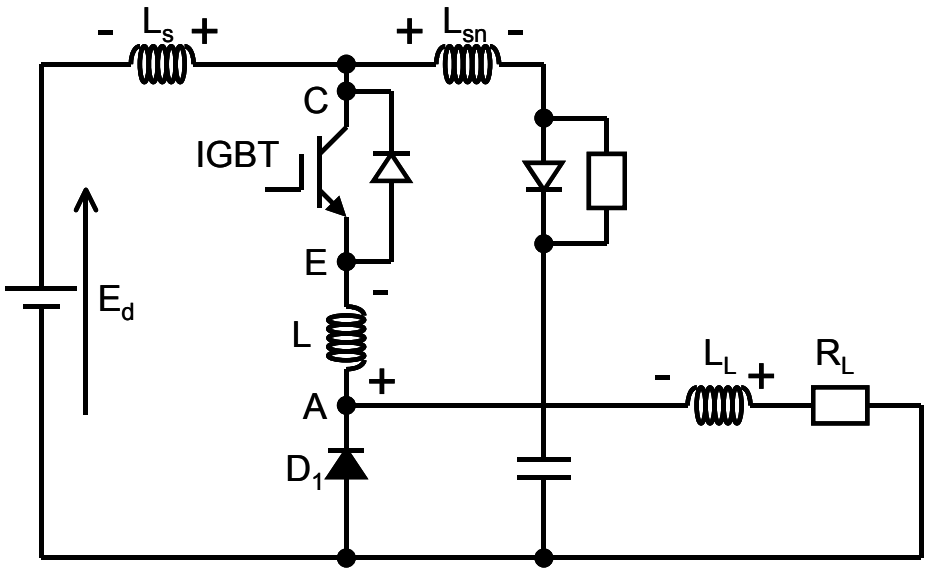


Fig. 9-2 Spike voltage measurement circuit

A voltage of the polarity shown in Fig.9-2 is induced in the circuit inductances during turn-off. Note that in cases where V_{CA} instead of V_{CE}, is measured at this point as an initial voltage, then a voltage lower than VCE by –L*di/dt will be erroneously measured.

(IV) Keep the probe measurement leads as short as possible.
(V) Keep probe leads away from high di/dt areas so that noise interferences are not picked up.

If the voltage probe is connected to the circuit under the IGBT, the reference potential of the oscilloscope would equal the switching circuit. If there is a large ground potential variation in the switching circuit, common-mode current would flow through the power line of the oscilloscope, causing its internal circuit to malfunction. Noise interferences can be verified, for example, by:

(I) Debating whether the standing wave can be logically explained.
(II) Comparing with wave forms observed on a battery-powered oscilloscope that is less susceptible to noise interferences.

(4) Gate voltage measurement (Gate-emitter voltage measurement)

Although the gate-emitter voltage, like the initial voltage, can be directly measured on an oscilloscope, care should be taken to prevent noise interferences during probe connection and disconnection. This is largely due to the high impedance of the signal source and the gate resistance connected in series with the gate of the IGBT.

The measurement deserves similar attention as in the initial voltage measurement.

2.3 Current measurement

Current probes are used for current measurement. Because practical devices have their main circuitry downsized to cut wiring inductances and simplify their geometry, the wiring needs to be extended to measure the device current. A current transformer can be used to minimize the wiring extension and thus to cut its effect as much as possible. The use of current transformers is also necessary to make up for the limited measuring capacity of the current probe.

A current probe maintains insulation from the conductive part to enable current measurement, but, in addition to being an electromagnetic induction-based detector, it has such a low signal level that it is susceptible to induction-caused noise interferences. Care should be taken, therefore, to guard against noise interferences.

(1) Current detectors

Table 9-2 lists examples of the current detectors.

Table 9-2 Current detectors

No.	Description	Model	Brand	Remarks
1	DC current probe Dedicated amplifier and power supply required	Model A6302	Sony Tektronix	Maximum circuit voltage: 500V Up to 20 A at DC to 50 MHz Up to a peak pulse current of 50A
2		Model A6303		Maximum circuit voltage: 700V Up to 100A at DC to 15MHz Up to a peak pulse current of 500 A
3	AC current probe	Model P6021		Maximum circuit voltage: 600V Up to 15Ap-p at 120Hz to 60MHz, Peak pulse current: 250A
4		Model P6022		Maximum circuit voltage: 600V Up to 6Ap-p at 935Hz to120MHz Peak pulse current: 100A
5	ACCT	Varied	Pearson	Less than 35MHz
6	AC current probe with a Rogowski coil	CWT	PEM	Current range: 300mA to 300kA Bandwidth: 0.1Hz to 16MHz

(2) Current probe sensitivity check

Before making any measurements, it is necessary to check the probe sensitivity. Use the calibrator output of the oscilloscope or use an oscillator to calibrate the current probe shown in Fig.9-3.

The measurement method of Fig.9-3 uses resistance R (No induced drag is used). Both voltage (e) and R is measured. This voltage (e) is divided by R and current (i) is obtained. These currents are compared with the shape of waves of the current probe and checked for accuracy. If the current (i) is too small, increase primary winding of the current probe.

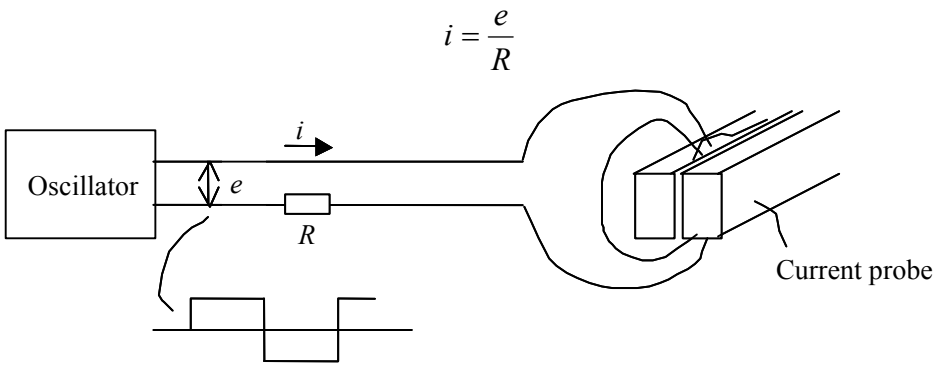


Fig. 9-3 Current probe calibration method

(3) Current measurement method

Fig.9-4 shows where current transformers (CT) are inserted to measure the current through a semiconductor device, and the method of current measurement with two devices connected in parallel.

When the current of T11 on the part of a positive arm is measured, the secondary side current of CT1 is measured with the current probe. Moreover, the current of T12 measures the side current of the second ditto CT2 with the current probe. The current of the positive side arm (total of the current of the current of T11 and T12) can be measured with the same current probe by measuring in bulk after the direction of the second side current of CT_1 and CT_2 is matched. Please refer to sections 9-6 and 9-7 for the application of the current probe and transducers.

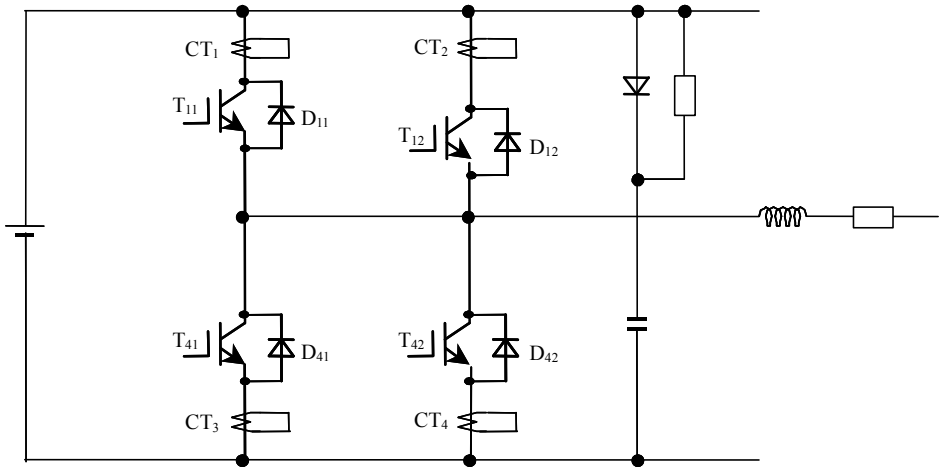


Fig. 9-4 Current measurement method

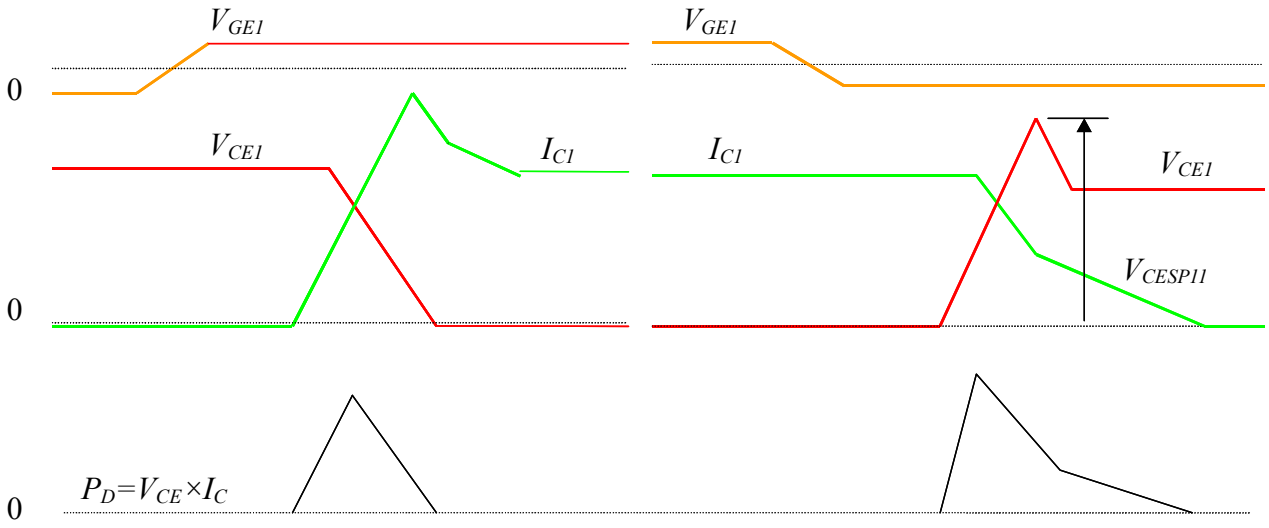
2.4 Switching loss measurement

The switching loss must be the loss generated between the two instants of time at which switching starts and at which the effect of switching is lost. The turn-on loss, for example, is the loss that is generated after the gate and source are forward-biased until the drain-source voltage reaches the saturation voltage. The switching loss is generally expressed in terms of the energy generated per instance of switching.

Fig.9-5 shows examples of switching waveforms and switching losses. Correct current and voltage waveform measurement is prerequisite to switching loss measurement. Note that when current and voltage are measured simultaneously, the common-mode current flowing from the voltage probe causes the current waveform to be distorted. The presence or absence of a common-mode effect can be determined by comparing the current waveforms associated with the availability and non-availability of voltage probes.

If the current waveform is distorted, insert common-mode chokes (cores with excellent high frequency characteristics having a cable wound on them) into the voltage probe and oscilloscope power cables as shown in Fig.9-6 to alleviate the distortion

Equally important is the settings of reference 0V and 0A. Note that, in current measurement operations using an AC current probe, the position of 0A varies depending on the measurement current value and the conduction ratio.



$$E_{on} = \int_{t0}^{t1} V_{DS} \times I_D \bullet\ dt \qquad E_{off} = \int_{t3}^{t2} V_{DS} \times I_D \bullet\ dt$$

Fig. 9-5 Switching losses

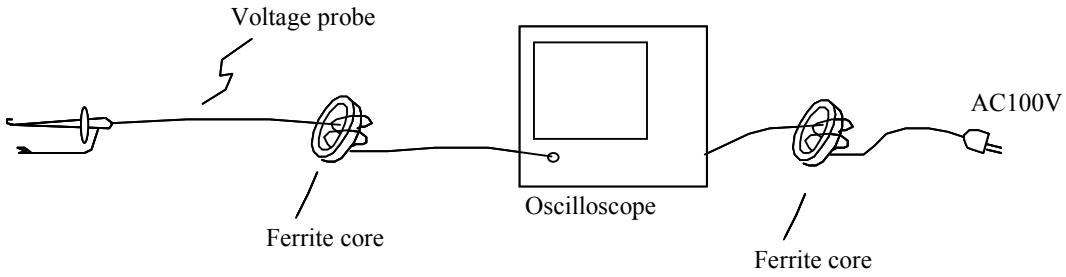


Fig. 9-6 Inserting common mode chokes

2.5 Selecting oscilloscopes

Because oscilloscopes vary in terms of functionality and performance, it is important to select the right oscilloscope to suit the measurement items required and the rate of change in the signal of interest. This section provides a summary description of the signal source rise time and the frequency bandwidth requirements for the oscilloscopes to be used.

(1) Relationship between the rise time of a pulse waveform and the frequency band

The rise time of a pulse waveform is defined as the time needed for the voltage to vary from 10% to 90% as shown in Fig.9-7.

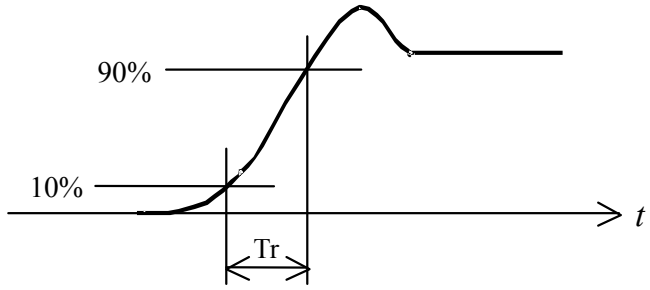


Fig. 9-7 Definition of the rise time of a pulse waveform

Assuming that the rise time is Tr and the frequency at which -3 dB is attained is F_{-3dB}, then the following relationship holds between them:

$$T_r \times F_{-3dB} = 0.35 \quad \cdots\cdots (1)$$

(2) Signal source rise time (T_{r1}) and oscilloscope selection

Fig.9-8 shows the rise time of each component of an actual system of measurement.

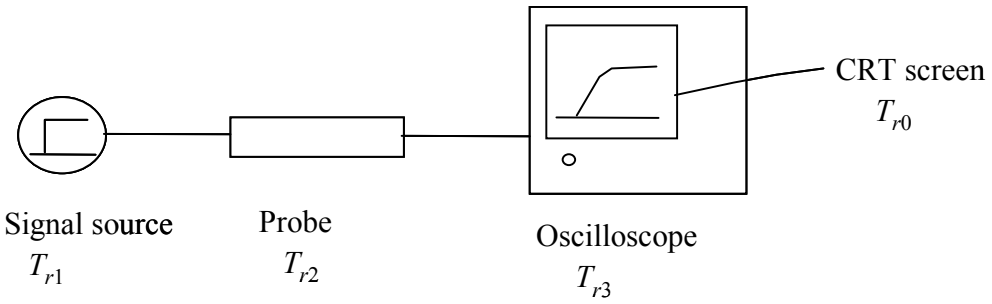


Fig. 9-8 System of measurement and component rise time

The rise time T_{r0} of the waveform displayed on the CRT screen of the oscilloscope is determined by the component rise time and is expressed as:

$$T_{r0} = \sqrt{T_{r1}^{\ 2} + T_{r2}^{\ 2} + T_{r3}^{\ 2}} \quad \cdots\cdots (2)$$

A correct reproduction of the waveform of the signal source is accomplished by setting $T_{r0} = T_{r1}$.
Assuming that:

$$\varepsilon = \frac{T_{r0} - T_{r1}}{T_{r1}} \times 100 \quad (\%), \quad k = \frac{T_{r2} + T_{r3}}{T_{r1}} \quad \cdots\cdots (3)$$

If Eq.(2) is used to determine the relationship between ε and k, it would be as tabulated in Table 9-3.

Table 9-3 Waveform measurement errors, and signal source and measuring apparatus startup time ratios

ε (%)	1	2	3
K	7	5	4

According to these relationships, the sum total of the probe and oscilloscope startup times must not exceed one fourth of the rise time of the signal source. (Exp. Tr0 = 3.5ns, ε = 3%, 3.5/4 = 0.87 ns)

If the startup time of the probe is disregarded, solving Eq. (1) gives the required frequency band of the oscilloscope as $0.35/0.87 \times 10^{-9} = 4 \times 10^{8}$, or 400 MHz. Accordingly, an oscilloscope having a frequency band of 400 MHz or above must be used.

Thus, the selection of the oscilloscope to be used should reflect the rise time of the signal of interest.

2.6 Selecting probes

Probes are available in two types as mentioned earlier: voltage probes and current probes.

This section provides basic hints on selecting probes and their usage tips.

2.6.1 Voltage probes

(1) Rise time

It is important to allow for a frequency band for the probe to be used that is in accordance with the rise time of the signal of interest as explained in 9.7. The concept of probe selection is similar to the concept of oscilloscope selection and is not defined here.

(2) Effects of the signal source impedance and probe capacitance on the rise time

An electrical equivalent circuit of the system of measurement is shown in Fig.9-9, in which R_1 and C_1 denote the output impedance and capacitance of the signal source, respectively, and R_2 and C_2 denote the input impedance and capacitance of the oscilloscope, respectively.

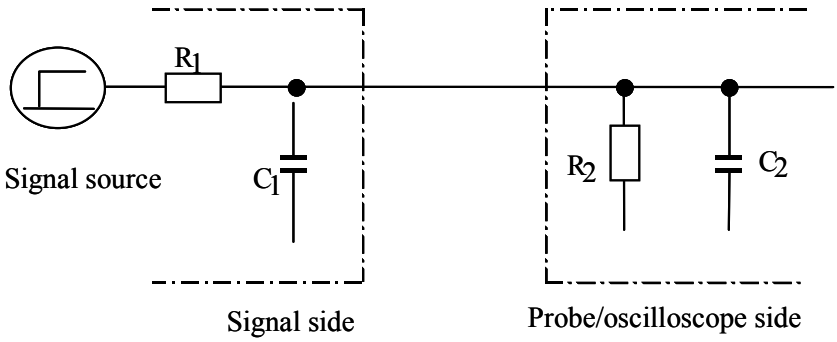


Fig. 9-9 Electrical equivalent circuit of the system of measurement

The rise time *Tr* of the C-R filter can be expressed by:

$$T_r = 2.2 \times R \times C$$

In Fig.9-9, R and C can be expressed in equations as:

$$R = \frac{R_1 \times R_2}{R_1 + R_2} \qquad C = C_1 + C_2$$

The following facts become apparent from these relationships:

1) The higher the output impedance of the signal source, the longer the rise time becomes.
2) This also holds true with probes or oscilloscopes having a large capacitance:

① For example, if the signal of a signal source (R1 = 500Ω, C1 = 2 pF) is measured using an ordinary passive 10:1 probe (C2 = 9.5 pF, R2 = 10 MΩ), a rise time of 12ns, would result from the connection of the probe, compared with 2.2 ns without its connection, generating a significant error.

(3) Probe selection

Table 9-4 summarizes the conditions for selecting probes to suit specific measurement objectives and tips on measurement using these probes.

Table 9-4 Conditions for selecting probes to suit specific objectives of measurement

Measurement / Item	Amplitude measurement	Rise time	Phase difference
Probe requirements	The input impedance must be high in the working frequency band.	A sufficient frequency band is available for the rise time of the signal source.	Low input capacitance Matched cable lengths and characteristics
Directions	The pulse width is at least five times the time constant of the probes and the oscilloscope. Select a signal source of the lowest impedance possible.	The pulse width is at least five times the time constant of the probes and the oscilloscope. Select a signal source of the lowest impedance possible.	Measure the probe-to-probe time difference beforehand. *A 3.5-feet probe has a delay of 5 ns.

(4) Directions

Correct signal measurement requires an understanding of the characteristics of probes to make a correct choice. Key items to consider when selecting a probe are listed below.

a. Does the probe have the current range to measure the desired target voltage/current.
b. Is the frequency bandwidth of the probe correct for the measurement?
c. Is the maximum input (withstand voltage) adequate?
d. Will the loading effect of the probe cause a false reading? (optimal measuring points)
e. Is the ground (earth wire) connected properly?
f. Are there mechanical or physical strains?

In measuring fast switching pulses, grounding should be checked carefully. In this case, resonance could arise from the inductance of the ground lead and the probe capacitance. Such resonance would be particularly pronounced in a broadband oscilloscope. Shortening the probe ground lead to ground and the tip can reduce resonance or oscillation. An adapter usually comes with each voltage probe as an accessory for this purpose.

In addition, a ground lead may be connected to each individual probe to guard against induction-caused noise interferences shown in Fig. 9-10. The points to which the ground leads are connected must have equal potentials in this case.

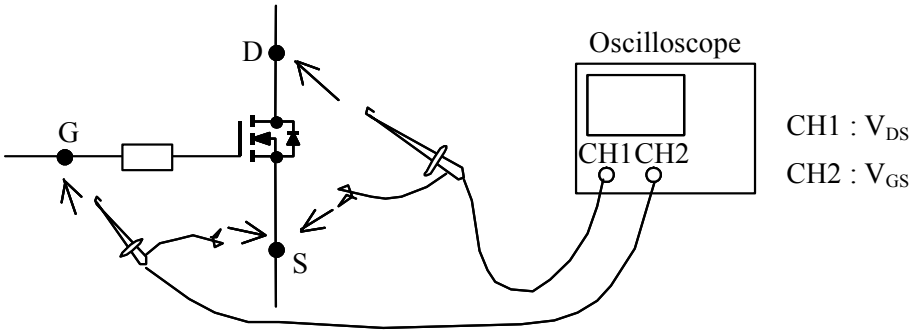


Fig. 9-10 Connecting voltage probes

2.6.2 Current probes

The types of current probes available are as described in 2.3. This section focuses on tips on using current probes in actual applications.

(1) Current probe selection

Current probes are available in two types as mentioned earlier: DC current probes and AC current probes. AC current probes, with their better noise immunity, are recommended for use in measuring current waveforms during fast switching action.

If a DC or low-frequency AC current is introduced through an AC current probe, the core in the probe would be saturated to suppress output. To measure the switching action of an IGBT used in a circuit that deals with a DC or low-frequency AC, some techniques are necessary, such as fabricating and using a timing control circuit to simulate the actual action.

(2) Use precautions

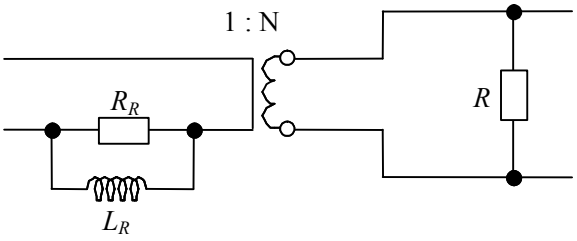
a. A ferrite core is housed in the tip of a current probe. The ferrite core is extremely vulnerable to impact and must be protected against dropping.

b. Be careful not to exceed the ratings.
   - Withstand voltage: If the circuit voltage is high, cover the measuring point with a voltage-resistant tube.
   - A-S (current product): Pulse current rating. Excessive current flow could cause damage to the probe.
   - Maximum RMS current immunity: Limited by the power capacitance of the secondary circuit in the probe transformer. The probe could be burned if this limit is exceeded.

c. With a voltage clamping circuit, perform measurement with the current probe being securely clipped to the circuit.

d. Do not release the secondary side of the circuit with the current probe clipped to the circuit. (Without a terminator in position, a high voltage could be generated on the secondary side.)

e. Insertion impedance
   Inserting the probe into position generates an insertion impedance on the primary side of the circuit. It is important to ensure that the insertion impedance does not affect the measuring object.
   Assuming that the probe is an ideal transformer, the insertion impedance can be expressed in Fig.9-1.



$$L_R = \frac{\text{Secondary inductance } (L)}{N^2}$$

$$R_R = \frac{\text{Secondary load resistance } (R)}{N^2}$$

Fig. 9-11 Probe insertion impedance

2.7 Using current transformers

A current transformer is used to ease the constraint on the working range of a current probe and to minimize the effects partial modifications made to measurement purposes may have upon circuit performance. For information on the locations where current transformers are inserted and instructions on how to measure current, see Fig. 9.3.

Assuming that the number of turns (secondary) of the transformer is N, and the primary current is I_1 and the secondary current is I_2, an ideal transformer would meet the relationship $I_2 = I_1/N$. With the excitation current taken into account, the relationship can be rewritten as:

$$I_O = I_1 - N \times I_2$$

The excitation current must be a small value because it creates a measurement error. Check the value of N with regard to the transformer, measure I_1 and I_2 and calculate I_0 from the equation above to make sure that the measurement accuracy is acceptable.

Next, check the direction of the current flow. Current flows through the secondary winding in such direction that a magnetic flux generated in the core by the primary current is canceled.

Be careful not to drop the ferrite core because it could be damaged.

Chapter 10

EMC Design of IGBT Module

CONTENTS

In this chapter, EMC measures when IGBT module is applied are introduced.

1 General information of EMC in Power Drive System

Recently EMC measures coping with European CE Marking and Japanese VCCI(Voluntary Control Council for Information Technology Equipment) standards are indispensable in designing power electronic equipments such as Power Drive System(PDS) and Uninterruptible Power Source(UPS) using IGBT modules.

EMC is Electro Magnetic Compatibility, which is classified into EMI (Electro Magnetic Interference) and EMS (Electro Magnetic Susceptibility). EMI is adverse effects of electronic devices on peripheral equipments, and it is also called Emission. There are two kinds of EMI, one is conducted emission which leaks to power line and the other is radiated emission radiated as electromagnetic wave. EMS means immunity performance of electronic devices against disturbance, such as electromagnetic wave, voltage sag, electrostatic discharge, EFT/burst and lightning surge from the surrounding and it is also called Immunity. These are simplified as shown in Fig.10-1.

Since IGBT modules turn on and off several hundreds of voltage and several hundreds of current in several hundreds nanoseconds, both conducted emission and radiated emission are easily generated due to high dv/dt and di/dt of IGBT module. It is important to reduce those emissions when designing power electronics equipments.

In this chapter, effects of switching on others (EMI characteristics), which tend to become troubles in the application of the IGBT module, and countermeasures are introduced.

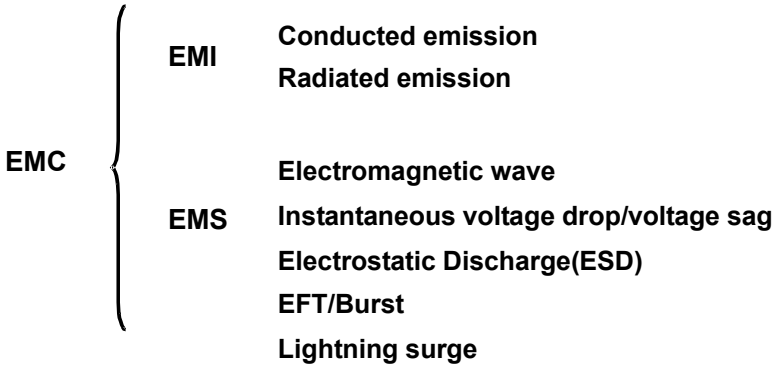


Fig.10-1 Classification of EMC

1.1 EMI performance

The IGBT module is used for equipments in a wide range of application field and power including such home appliance as air-conditioner and refrigerator, automobile and traction system as well as industrial PDS. Here are EMI standards related to PDS including general-purpose motor drive which is one of main application of the IGBT module.

(1) Conducted emission

In IEC61800-3, the limits (QP (Quasi-Peak) values) of the conducted emission are stipulated as shown in Fig.10-2 for PDS (Power Drive System).

The limits in the standard are classified into Category (C1) applied for equipments used in commercial area and Category (C2, C3) applied for equipments used in industrial area, and the industrial PDS are so designed as to clear Category C3 limits.

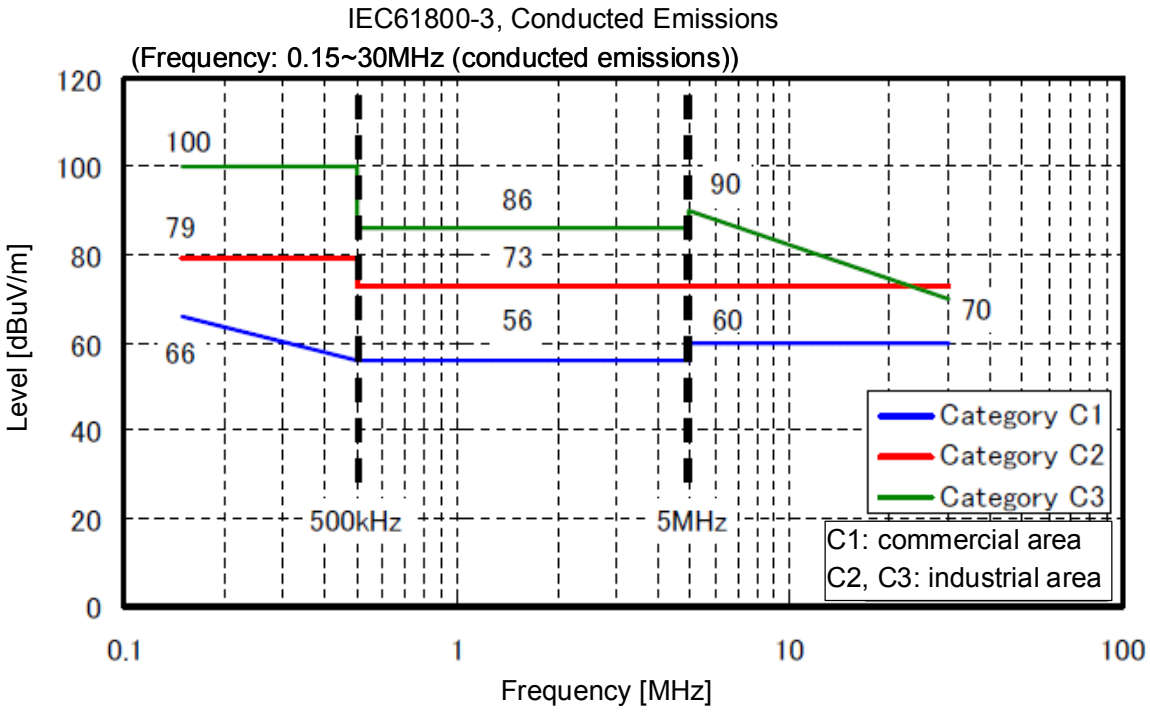


Fig.10-2 Limits of Conducted Emissions in IEC61800-3

(2) Radiated emission

Fig. 10-3 shows the standard limit values of radiated emission for each category. The category classification is defined as Fig. 10-4.

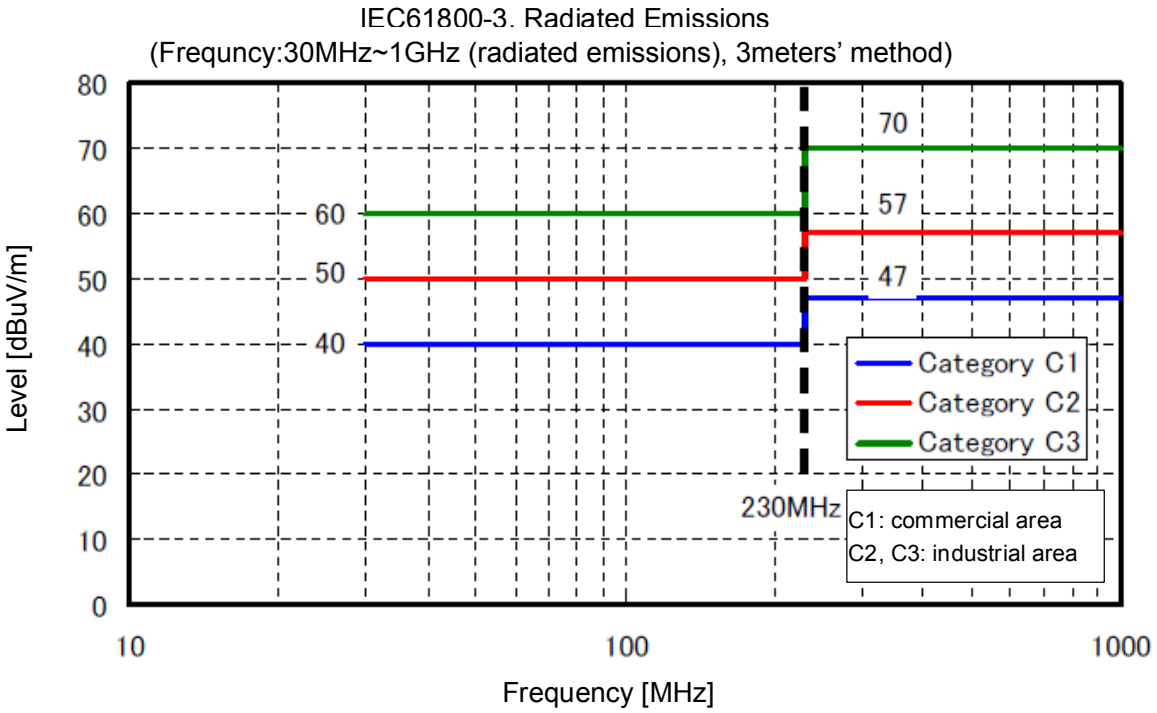


Fig.10-3 Limits of Radiated Emissions in IEC61800-3

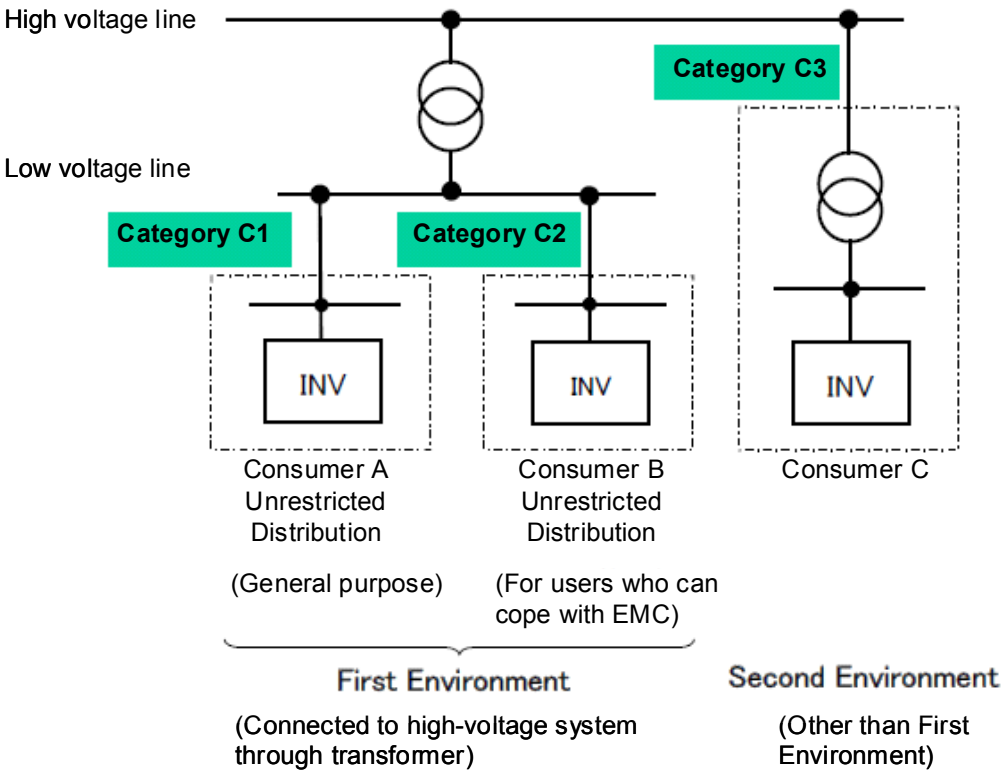


Fig.10-4 Category Classification in IEC61800-3

2 EMI design in Power Drive System

2.1 Common mode and normal mode noise

The propagation path of conducted emission is mainly classified into two types, normal mode and common mode.

The normal mode noise is generated by high dv/dt and di/dt due to switching of IGBT, is propagated in the main circuit and appears as noise at AC input terminal and output terminal. The path of the normal mode noise is shown in Fig. 10-5

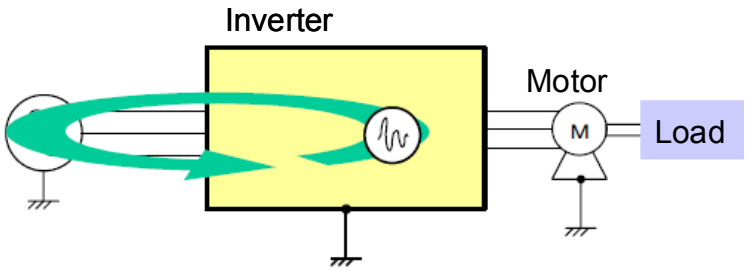


Fig.10-5 Path of Normal Mode Noise

On the other hand, the common mode noise is generated by potential fluctuation against ground due to charge and discharge of stray capacitance existing between main circuit and ground and in the transformer, and noise current is propagated through the ground line. The path of common mode noise is shown in Fig. 10-6.

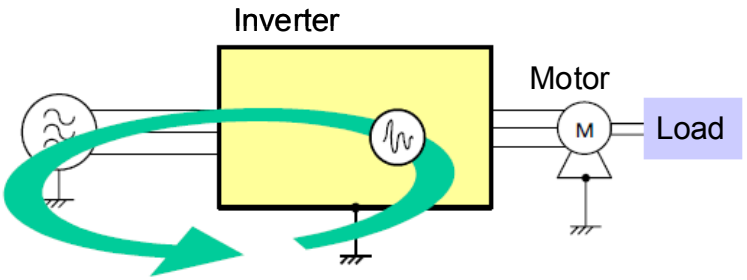


Fig.10-6 Path of Common Mode Noise

With actual equipment, there is impedance imbalance in the wirings of phases (e.g. R/S/T phase), and so the normal mode noise is changed to the common mode noise via the ground line (Fig. 10-7) or reversely the common mode noise is changed to the normal mode noise. In actual noise spectrum, therefore, it is very difficult to separate the noise through the normal mode path and the noise through the common mode path. As general caution, it is necessary to prevent the imbalance as much as possible for the phase wirings.

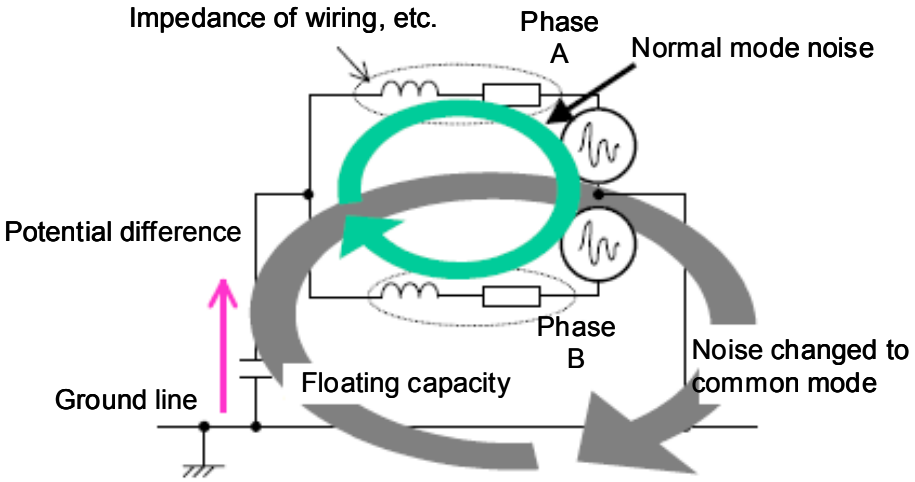
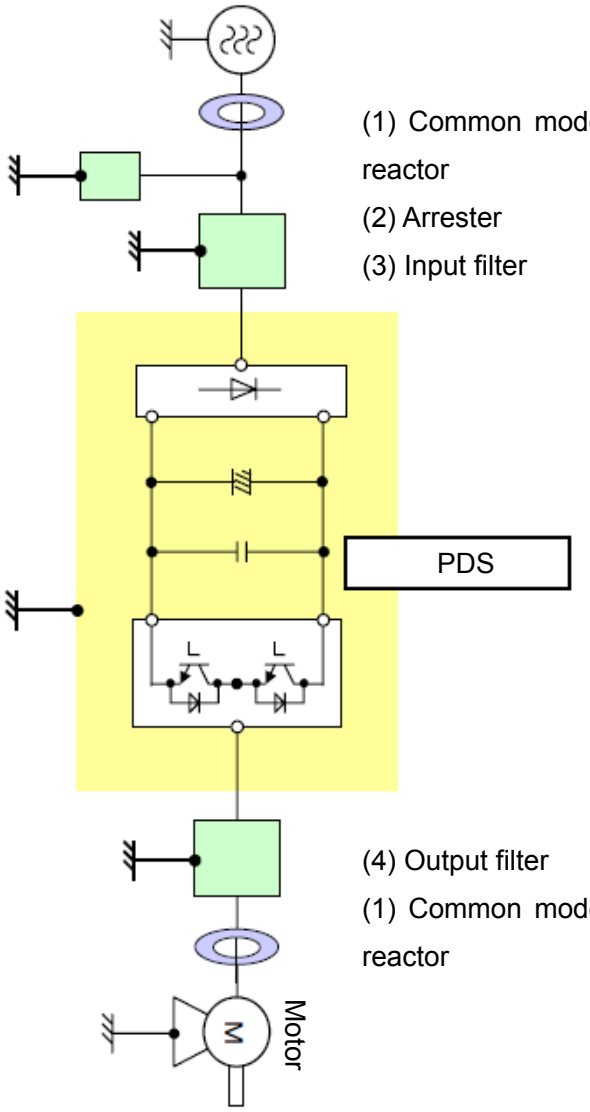


Fig.10-7 Path of Common Mode Noise

2.2 Measures against EMI noise in PDS

Fig. 10-8 shows general measures against noise in Power Drive System (PDS).

It is possible to control noise (mainly harmonics current and conducted emission) occurring in PDS by inserting such countermeasure parts as commercial noise filter and reactor.



The effects of the parts are as follows.

(1) Common mode reactor
This is a reactor of the common mode to be inserted in the input/output line. It is effective for controlling noise up to the band of several MHz.

(2) Surge protective device(Arrester)
This is installed to protect the PDS from induced common mode and normal mode lightning inflowing from the input power line.

(3) Input filter
This, composed of L and C, R, controls noise out flowing to the input power line. Various products having different noise attenuation characteristics are available in the market and proper selection should be made in accordance with the specification and purpose.
Since attenuation effect may be inferior depending on the installation method, proper wiring and installation are required in accordance with the instruction manual.

(4) Output filter
This is used for controlling surge voltage applied to the motor and controlling noise induced from the output cable.

Fig. 10-8 Measures against Noise of PDS

Such filters as described above to be installed outside the PDS are effective for noise control in the bands of 100kHz to several MHz, but may be less or not effective for higher bands (conducted emissions of 10MHz or higher and radiated emissions of 30MHz or higher).

This is because the frequency characteristics of filters are limited, and in order to effectively control emissions over a wide range of frequency, it is necessary to install optimum filters to meet the respective frequency.

2.3 Occurrence mechanism of emission attributable to module characteristics

One of factors to cause emission near the range of 10MHz to 50MHz is wiring inductance and/or stray capacitance around the IGBT module in the PDS, and it is considered that resonance occurs accompanying switching. In this section, the mechanism of emissions occurring around the IGBT and the countermeasures are introduced.

Fig. 10-9 shows the block diagram of a typical power drive system. In this figure, AC power source is rectified into DC by rectifier diodes and then reversely converted into AC by switching at high frequency the IGBT of the inverter portion, thereby achieving variable speed driving of the motor. The IGBT module and rectifier diode are mounted on a cooling fin, and this cooling fin is a part of a PDS body and is normally grounded for safety.

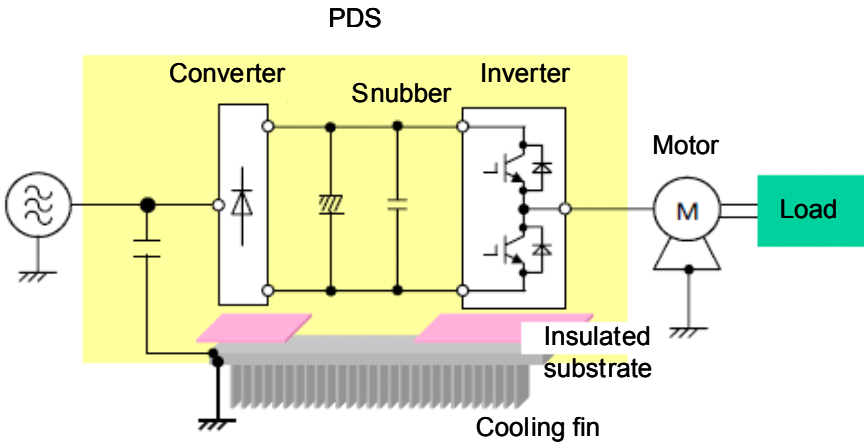


Fig.10-9 Path of Common Mode Noise

In this system , the metal base of IGBT module mounted on a cooling fin and the electric circuit side such as IGBT chip are insulated each other by a highly thermal conductive substrate. (For the detailed structure of the module interior, see Chapter 1)

A snubber capacitor which suppresses surge voltage is connected to the IGBT of the inverter portion.

In the area of MHz order such as radiated and conducted emission, however, the wiring inductance, stray capacitor which are not appeared on circuit diagram may give large effects.

Fig. 10-10 shows a schematic diagram of PDS in such high-frequency bands as hundreds of kHz to tens of MHz. At a high frequency, stray capacitance and stray inductance existing in IGBT module and electrical parts give a very large effect. On the wiring around IGBT module, tens to hundreds nano henry of stray inductance may exist, and on the insulating substrate described above, hundreds pico farad of stray capacitance exists. There exists Junction capacitance at the PN junction of the IGBT itself.

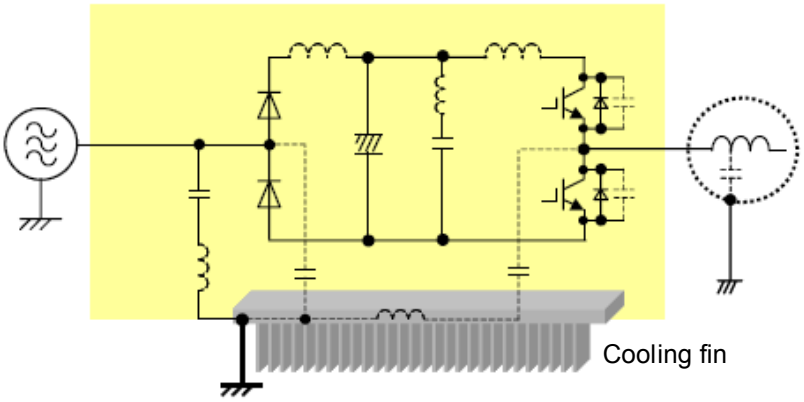


Fig.10-10 Equivalent Circuit Considering Parasitic L/C

Assuming, for example, that the stray inductance of the wiring is 200nH and the stray capacitance of the substrate is 500pF, and if they are looped, the resonance frequency fo of the loop is calculated as Fig. 10-11.

$$fo = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{200\text{nH} \times 500\text{pF}}} \fallingdotseq 16\text{MHz}$$

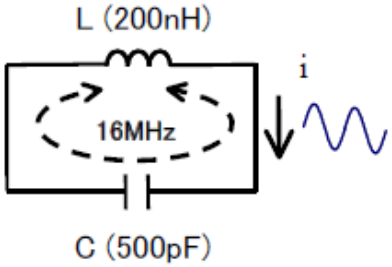


Fig.10-11 Resonance phenomenon between stray inductance and stray capacitance

If switching of IGBT becomes a trigger and the resonant current of 16MHz flows in the loop, the resonant current will generate conducted emission and radiated emissions. In the case shown in Fig. 10-10 common mode noise current of 16MHz via the insulated substrate of IGBT module flows out to the ground line, and it is propagated to the input power line and appears as the peak of conducted emissions. If this resonance frequency becomes 30MHz or higher, it is observed as radiated emissions.

Table 10-1 shows an example of stray capacitance and inductance values of circuit components.

Table 10-1 Example of stray Capacitance and Inductance values in components of PDS

Circuit Components	Stray Capacitance	Stray Inductance	Remarks
Between P and N terminals of IGBT module	—	20~40nH	
IGBT chip	100~200pF	—	Voltage dependency is large
Snubber capacitor		20~40nH	
Insulated substrate	500~1,000pF	—	
Electrolytic capacitor	100pF	—	Between internal electrode and mounting metallic band
Iron-core reactor	50~200pF	—	At several MHz or higher a reactor works as a capacitor.
Varister	100~200pF	—	The higher voltage resistance is, the smaller stray C is.
Motor	13,000pF	—	Example of 3-phase 15kW induction motor
Shielded 4-core cable	Hundreds of pF	Hundreds of nH ~several micro H	Per meter
Wiring busbar	—	Hundreds of nH	About 100nH per 10cm

In an actual system, these components are connected in a complicated way, and an unintended L-C resonance circuit will be formed. Due to the IGBT switching, resonance current will be occurred in the L-C circuit and will generate peak value of conducted emission and radiated emission.

Table 10-2 and Fig. 10-12 show resonance loops that tend to cause the peaks in the conducted and radiated emissions.

Table 10-2 Example of Resonance Loops in PDS

	Frequency	Conducted/radiated	Normal/common	Path
(1)	1~4MHz	Conducted	Common	Motor capacitance ~ wiring inductance
(2)	5~8MHz	Conducted	Common	DBC substrate capacitance and wiring inductance
(3)	10~20MHz	Conducted	Common	DBC substrate capacitance and wiring inductance
(4)	30~40MHz	Radiated	Normal	Device capacitance ~ snubber capacitor

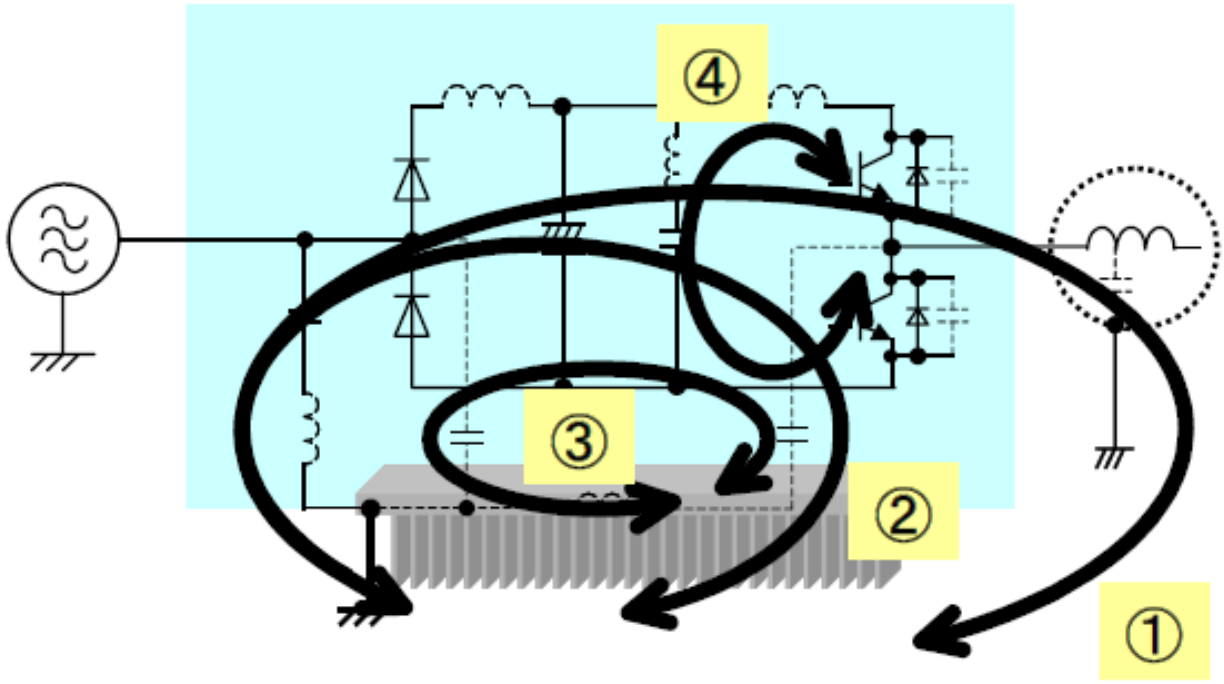


Fig.10-12 Example of Resonance Loops in PDS

The wire length (inductance) and stray capacitance vary depending on the system configuration, but approximate resonance frequency can be estimated by roughly calculating inherent stray L and C values in a subject system.

2.4 Frequency bands affected by IGBT module characteristics

As aforementioned, the frequency of the conduction noise for a power drive system such as general-purpose motor drive is 150kHz ~ 30MHz. Fig. 10-13 shows an example of measured data of the conducted emissions in PDS. As shown in Fig. 10-13, the conducted emission is highest near 150kHz, and as the frequency becomes higher, it is mildly attenuated. In the spectrum of the conducted emissions, the harmonics of rectangular switching waveform at the carrier frequency (several kHz ~ 20kHz) appears, and therefore, it is hardly affected by the switching characteristic of the IGBT module itself. This is because, as shown in Fig. 10-14, the voltage rise time and fall time in the switching of IGBT module are about 50~200 nanoseconds which is equivalent to 2~6MHz in terms of frequency, and in the frequency band lower than this, spectrum of conducted emission does not depend on the rise time and fall time of IGBT module.

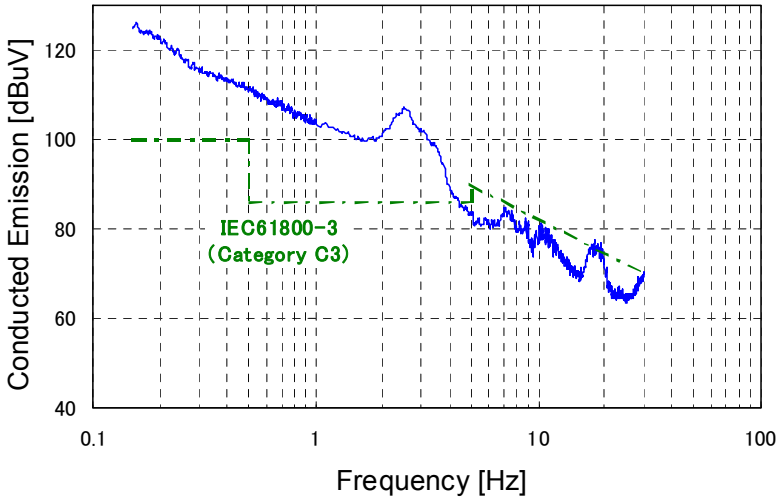


Fig.10-13 Example of Conducted Emission of PDS

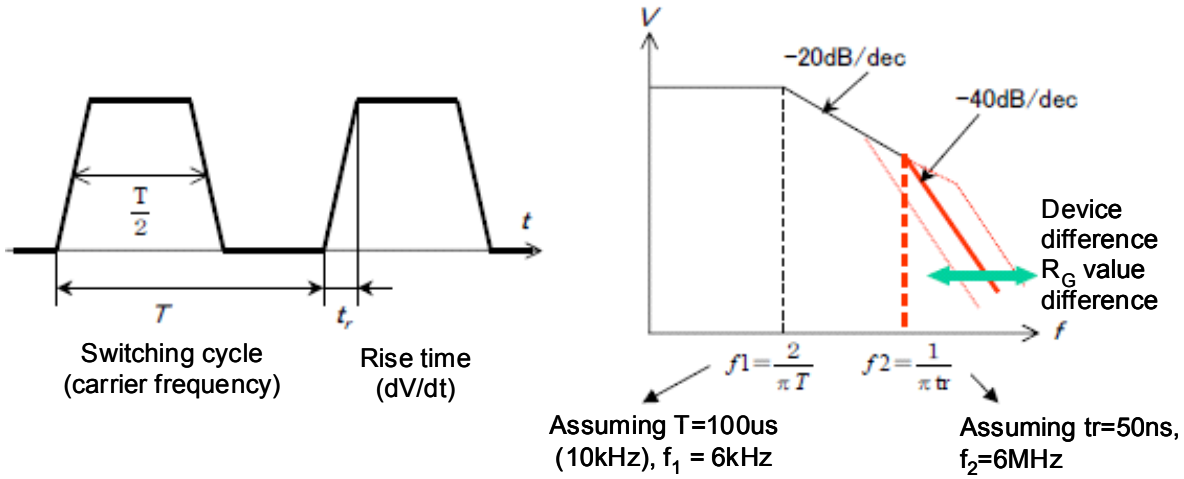


Fig.10-14 IGBT Voltage Waveform and Frequency Spectrum

Fig. 10-15 shows measurement results of radiated emissions (30MHz ~). Like the conducted emissions, the radiated emissions become the highest near 30MHz, which is the lowest frequency of the standard, and tend to attenuate as the frequency becomes higher. As shown in Fig. 10-15, the noise spectrum due to switching of IGBT does not have a sharp peak such as the CPU clock but a relatively broad.

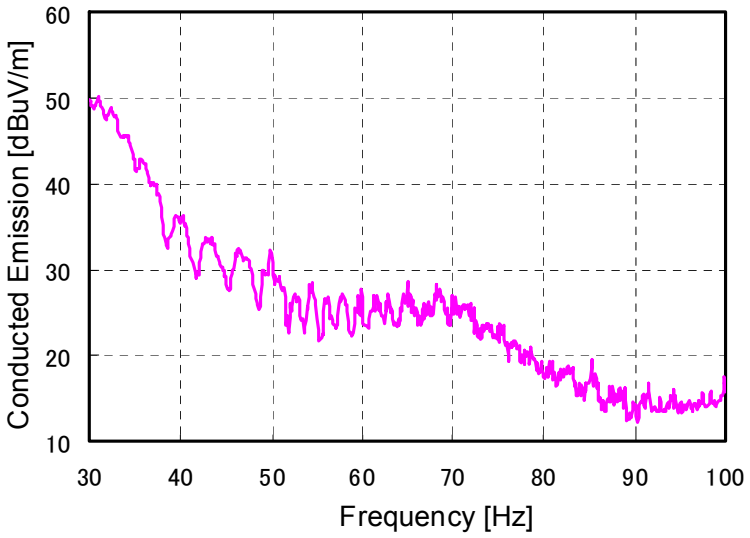


Fig.10-15 Radiated Emission Spectrum of 7MBR100U4B120 with Standard Gate Drive

3 EMI countermeasures in applying IGBT module

3.1 Measures against conducted emissions

3.1.1 Filter installation

Normally as the measures against the conducted emission, an input filter is installed on the input AC side to prevent the noise current produced in the inverter from out flowing to the AC power line. The input filter is composed of L and C elements, and the cutoff frequency of the filter is so designed that sufficient attenuation will be obtained for the target standard value. Since various filters for preventing emission are marketed by magnetic material and capacitor manufactures, a proper one should be selected in accordance with the relevant standard and necessary input current.

Fig. 10-16 shows reducing effects of an input filter designed for Category C2 of IEC61800-3. The conducted emission that was about 125dBμV at 150kHz without filter was attenuated to 70dBμV thanks to the filter, thus clearing the standard value with the margin of several dBμV.

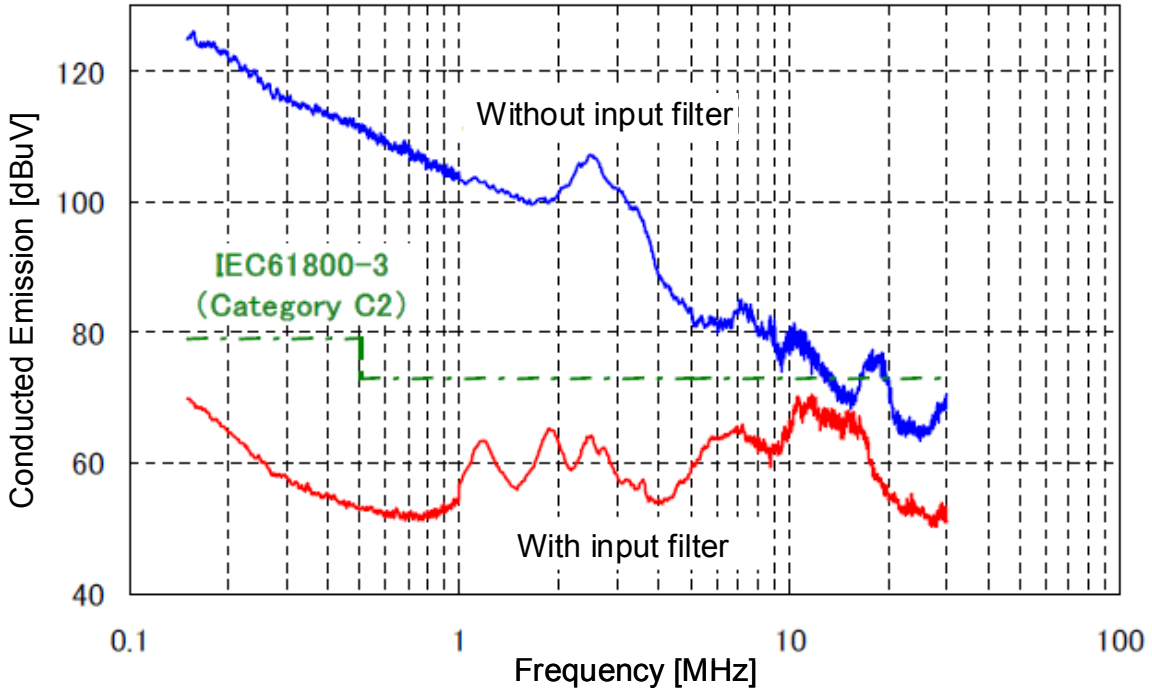


Fig.10-16 Measurement Results of Conducted Emissions in 3-Phase PDS 200V/37kW (QP Value)

3.1.2 Cautions when filter is applied

In case of an ideal filter, the attenuation becomes large as the frequency increases, but in actual filter circuits, ideal attenuation characteristic can no more be obtained at a certain frequency or higher, as shown in Fig. 10-17. This is because, as aforementioned, stray L and C exist in parts used for the filter circuit, and the attenuating effect tends to decrease at the frequency of 1MHz or higher, like the measurement results of conducted emissions shown in Fig. 10-16.

Furthermore, the peak appears in a high frequency band near 10MHz, and so the margin against the standard is the smallest. Depending on the measuring environment, the level near 10MHz may rise and exceed the standard value.

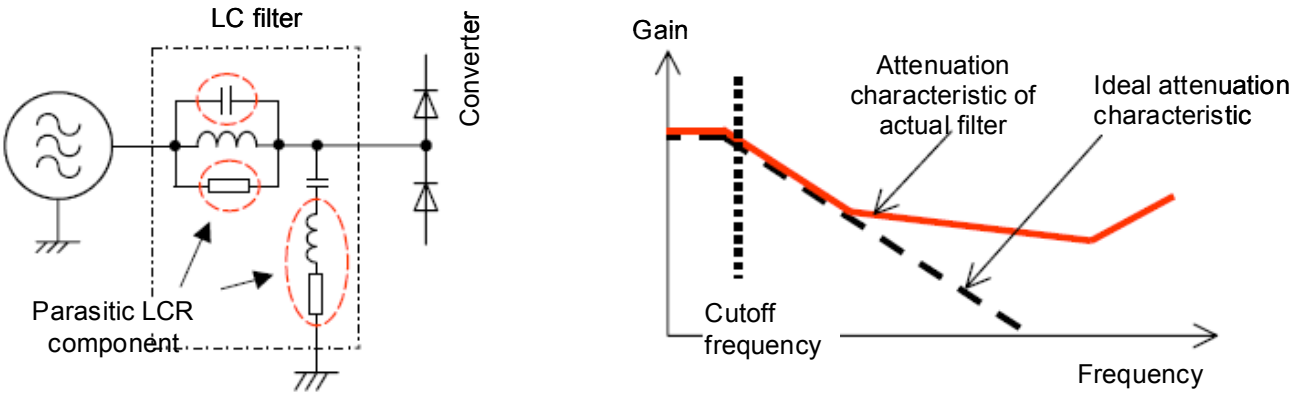


Fig.10-17 Attenuation Characteristics of Ideal Filter and Actual Filter

As one factor of the peak appearing in the band of 10MHz or higher of the conducted emissions, described in the preceding section, the resonance via the insulating substrate of the IGBT module can be cited.

Assuming, for example, that stray capacitance of the insulating substrate and stray inductance of main circuit are such values as shown in Fig. 10-11, the peak value of conducted emissions appears at 16MHz. The LC values of a loop that resonates with the frequency of 10MHz or higher are in the order of hundreds of pF and hundreds of nH, and the causes may be the capacitance of IGBT chip, insulating substrate capacitance and wiring inductance inside the package.

Fig. 10-18 shows an example of common mode circuit model of resonance via the DBC (Direct Bonding Cupper) substrate.

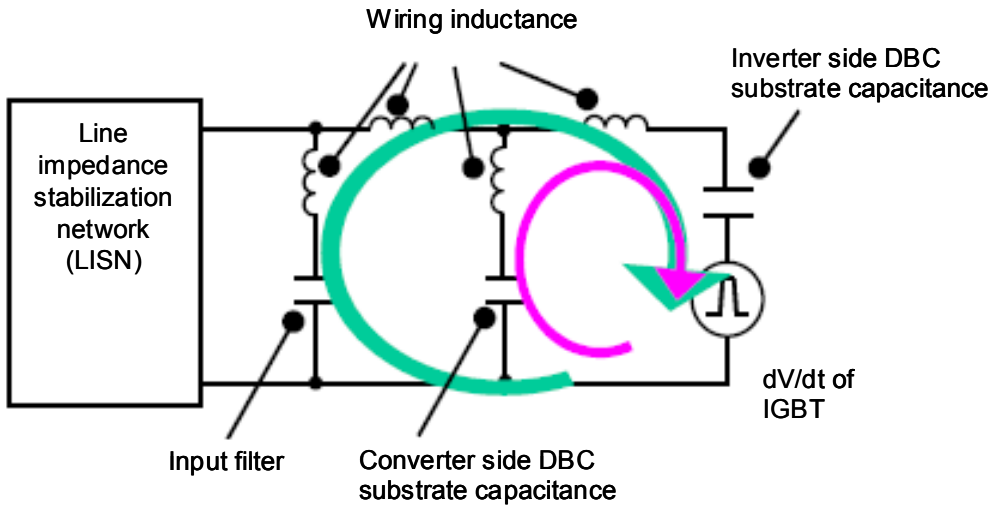


Fig.10-18 Example of Circuit Model of Resonance via Insulating Substrate of IGBT

This shows the resonance between the inductance of capacitor connected as an input filter and the substrate capacitance of inverter side module and the resonance between converter and inverter modules. When the filter or varistor is added to prevent emissions, it should be noted that the peak may appear due to the resonance with the parasitic L/C of the filter.

3.1.3 Measures against conducted emissions caused by IGBT module

In order to reduce the peak occurring in the high-frequency band of conducted emissions spectrum as described above, it is necessary to:

[1] to decrease dV/dt of IGBT for switching

[2] to make resonance current smaller by raising the impedance the resonance loop

But there are such demerits as shown below.

[1] IGBT loss will be increased when dV/dt is decreased.

[2] Only increasing/decreasing the constants of L and C will result in moving the resonance frequency, and it is difficult to decrease the peak value. It is impossible to eliminate the stray L and C components structurally and physically.

3.1.3.1 A measure of conducted emissions by adjusting gate resistance

Fig. 10-19 shows an example of conducted emissions spectrum of PDS (with input filter) applying 7MBR75U4B120. From Fig. 10-19, it is known that the peak near 10MHz of the conducted emissions is controlled about 5 dBμV when the gate resistance is 2 times or 3 times as big as standard value.

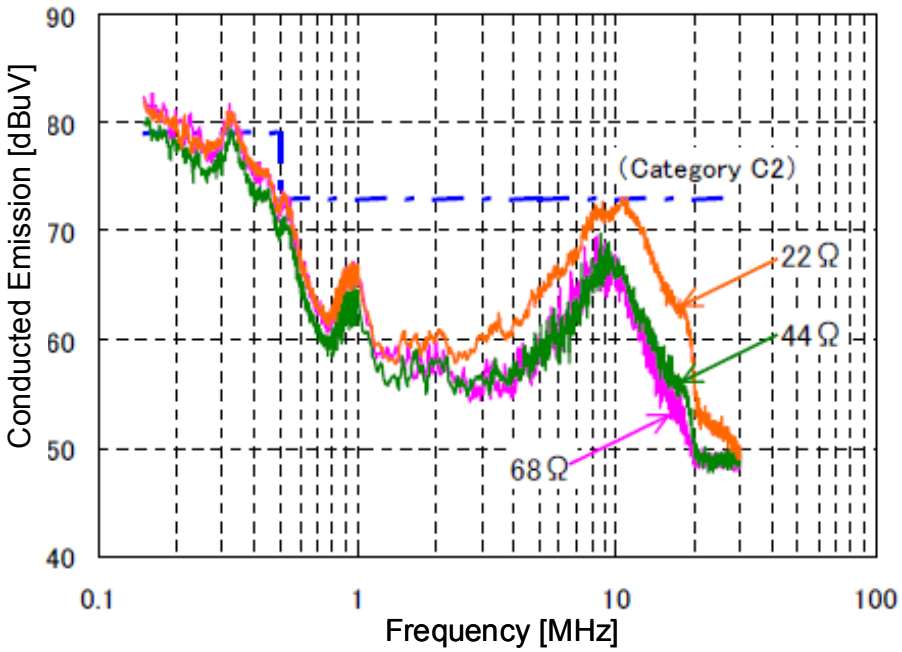


Fig.10-19 Measurement of Conducted Emissions of 7MBR75U4B120

Even if the gate resistance is increased to 2 times or more, the reducing effect is smaller, and so it is necessary to judge the reducing effect considering the demerit of increased switching loss.

3.1.3.2 Controlling of resonance with ferrite core

The ferrite core is one of parts often used for reducing the emissions. Its equivalent circuit is normally shown as a series circuit of L and R. The characteristics of L and R as magnetic material of the ferrite core are as shown in Fig. 10-21.

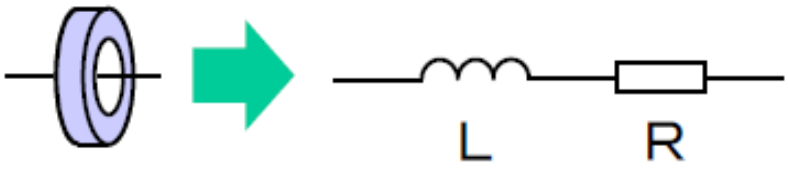


Fig.10-20 Equivalent Circuit of Ferrite Core

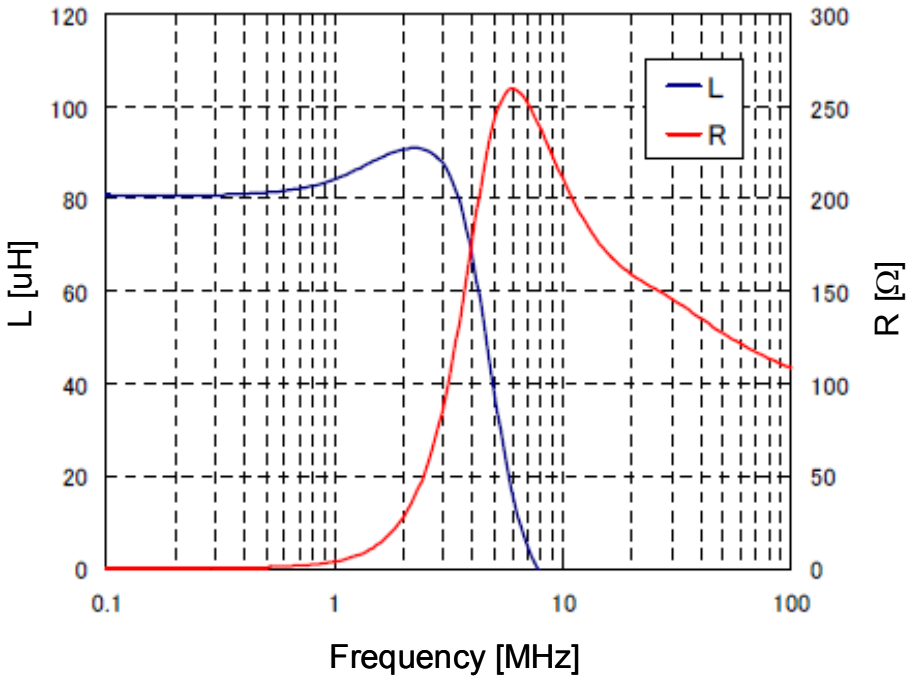


Fig.10-21 Impedance (L, R) Characteristics of Ferrite Core

If this ferrite core is inserted in the resonance loop to produce the noise peak described above, the following circuit model is made.

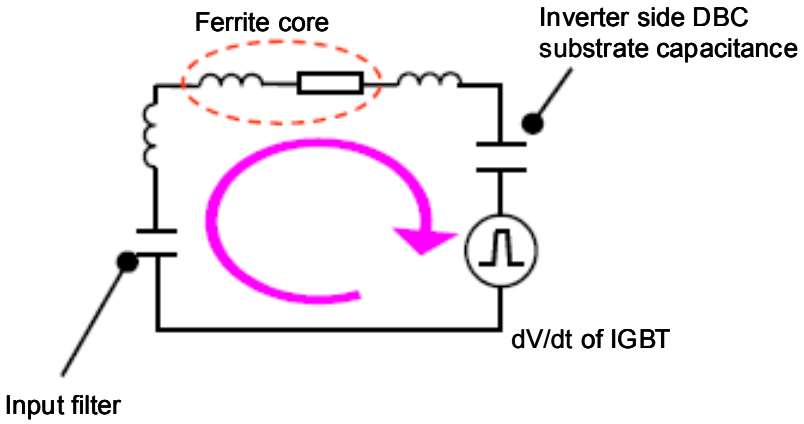


Fig.10-22 Equivalent Circuit When Ferrite Core Is Installed

By selecting a ferrite core material with optimum impedance characteristic in accordance with the constant (resonance frequency) of the loop, it becomes possible to control the noise peak by damping the resonance.

Fig. 10-23 shows the impedance characteristic of the resonance loop before and after the core measure is taken. At the resonance point, the impedance becomes the lowest and large resonance current runs, and so the peak occurs in the conducted emissions. By inserting the core here, the impedance is increased, and by damping the resonance, the conducted emissions can be effectively controlled.

Fig. 10-24 and Fig. 10-25 show an example of inserting the common mode/ferrite core in the PDS main circuit and reducing effects, respectively.

Since the loop impedance when no measure is taken is about 8Ω, peak reduction of about 10dB can be achieved by increasing it to about 30Ω by means of the ferrite core.

Unlike the gate resistance method, applying the core can reduce the emissions without increasing the loss of IGBT. In Fuji's 5th generation IGBT modules, U4 series, the tradeoff between high-speed switching and low-noise characteristic is greatly improved when a core is applied. Furthermore, lower noise of equipment can be achieved without sacrificing the high-speed switching characteristic by arranging the ferrite core effectively. (Various patents are applied)

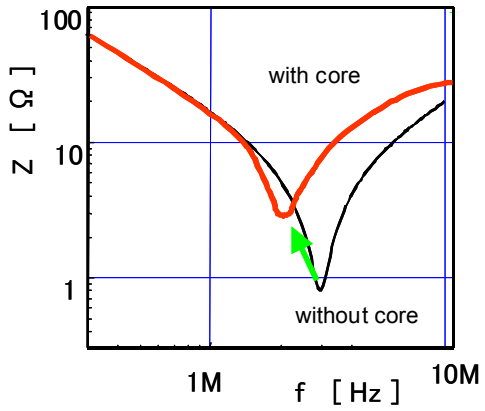


Fig.10-23 Impedance Characteristic of Resonance Loop before and after

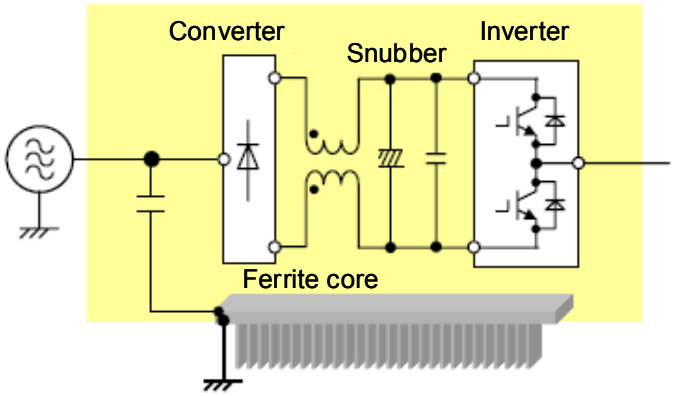


Fig.10-24 Example of Measure by means of Common

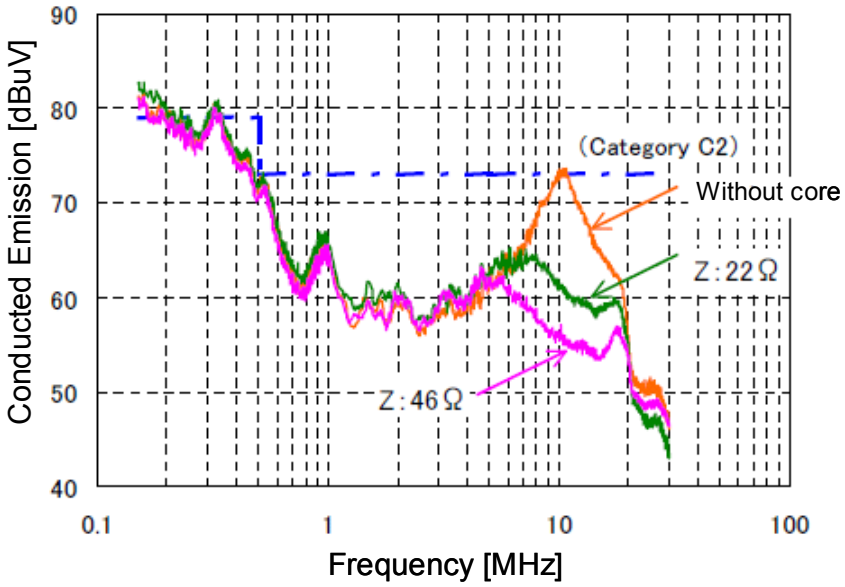


Fig.10-25 Measurement Results of Conducted Emissions

3.1.4 Measures against radiated emissions of IGBT module

The main cause of the radiated EMI emissions is considered to be the high-frequency L-C resonance produced by the junction capacitance of a semiconductor chips and stray inductance on the wiring (mainly the wiring between a module and a snubber capacitor) that is triggered by high dV/dt produced when the IGBT turns on (a FWD on the opposing arm side acts as reverse recovery) (Fig. 10-26). This is the same occurrence mechanism as the peak in the conducted emissions described above.

Generally, the far electric field Ef at frequency f radiated from a very small current loop (aforementioned L-C loop here) placed in a free space is given by the following formula (Maxwell's equations).

$$Ef = \frac{1.32 \times 10^{-14}}{\mathrm{r}} \cdot \mathrm{S} \cdot \mathrm{If} \cdot \sin\theta \qquad (1)$$

r: distance from loop, S: area of loop,
If: current value of loop, θ: angle from loop surface

Radiated emission

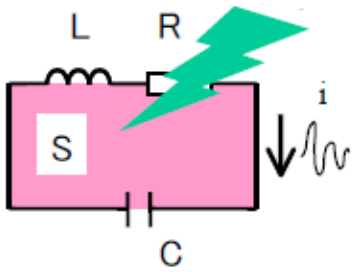


Fig.10-26 Loop formed by a module

From this formula (1), it is known that the Ef is in inverse proportion to the distance from the loop and the loop area is proportional to the loop current.

The current value If is given by the following formula.

$$If = \frac{E}{Z} \qquad (2)$$

E: voltage spectrum of switching waveform of IGBT (Fig. 10-14), Z: impedance of loop

In order to reduce the radiated emissions, therefore, the following measures may be considered.

[1] Increasing the distance from the loop
[2] Decreasing the loop area S
[3] Decreasing the loop current
- [3]a Decreasing the spectrum of switching voltage
- [3]b Increasing the loop impedance

As for [1], the measurement at the distance of 10m or 3m is specified in the standard, and therefore, realistic measures are [2] or [3].

3.1.4.1 Reducing loop area S

As described above, the high-frequency noise current induced when switching is the parasitic capacitance of the device and the resonance current of L-C loop formed by the snubber capacitor (path [4] of Fig. 10-12). With medium/large capacity module of 2in1 package class, it is necessary to minimize the radiation area of the loop by screwing the mold type snubber capacitor directly to the terminals. This is also effective from the viewpoint of controlling the spike voltage when switching.

Pin terminal type modules such as 6in1 and 7in1 types are installed on the power substrate in most cases, but it is important for the snubber capacitor to be arranged near the P/N terminal pins as much as possible.

3.1.4. 2 Decreasing voltage spectrum

As described above, the spectrum of voltage waveform when IGBT and FWD chips are switching is as shown in Fig. 10-27.

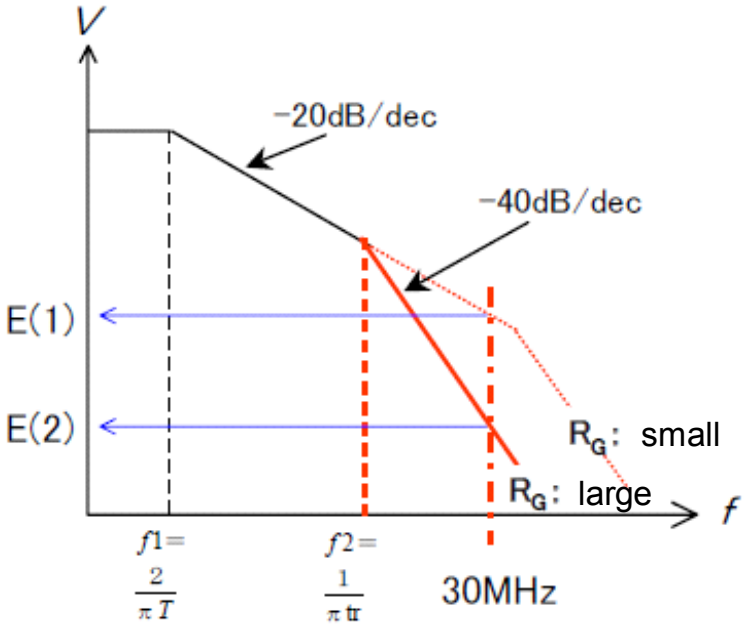


Fig.10-27 Spectrum of IGBT Switching Voltage Waveform

Conventionally, the method to make the rise time tr slower by increasing the gate resistance has been generally applied, and this means to make lower frequency of f2 in Fig. 10-27 and reduce the spectrum of 30MHz or higher. In comparison with the voltage component E(1) at 30MHz when RG is small and the voltage rise and fall time are short (dV/dt is large), the voltage component when RG is large and dV/dt is small becomes smaller like E(2).

Since E(1), E(2) is equivalent to E in Formula (2), reducing the dV/dt means to control the noise current If consequently.

Fig. 10-28 shows the dependency on gate resistance of the radiated emissions of 7MBR100U4B-120. By approximately doubling the standard resistance, the radiated emissions can be greatly controlled. Thus, the radiated emissions can be easily controlled by adjusting the gate resistance for U4 series, and the emission and loss are balanced well.

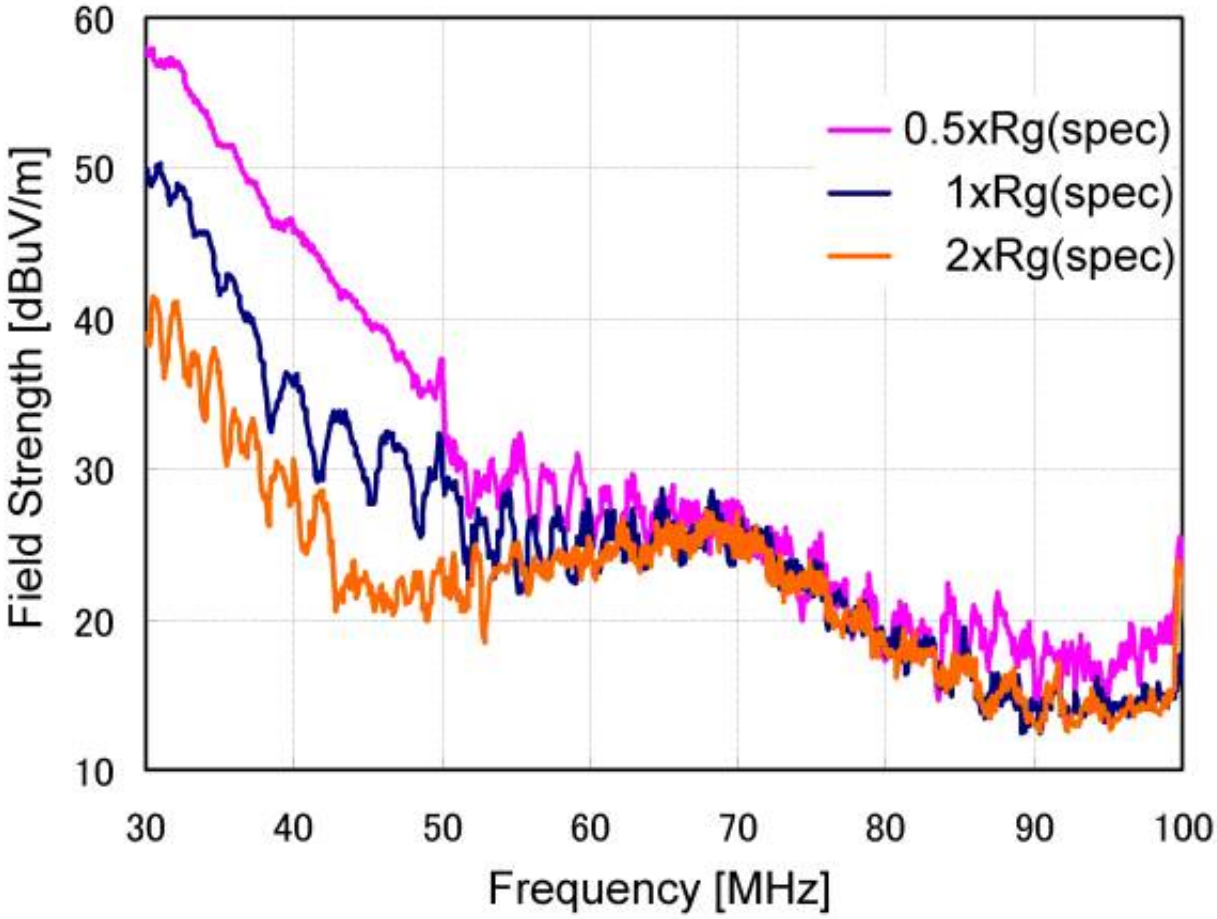


Fig.10-28 Dependency on Gate Resistance of Radiated Emissions of 7MBR100U4B-120

3.1.5 Summary

As described above, the EMI (especially the peak value of high-frequency conducted emission at not less than 10MHz and radiated emission) produced by IGBT switching is generated by the resonance of stray L and C existing in the IGBT itself and on its peripheral circuit. These stray L and C components cannot be reduced to zero in principle and physically. As the measures against the emissions, therefore, it is important to accurately discover the resonance of the loop to be the problem and take proper measures.

Chapter 11

Reliability of power module

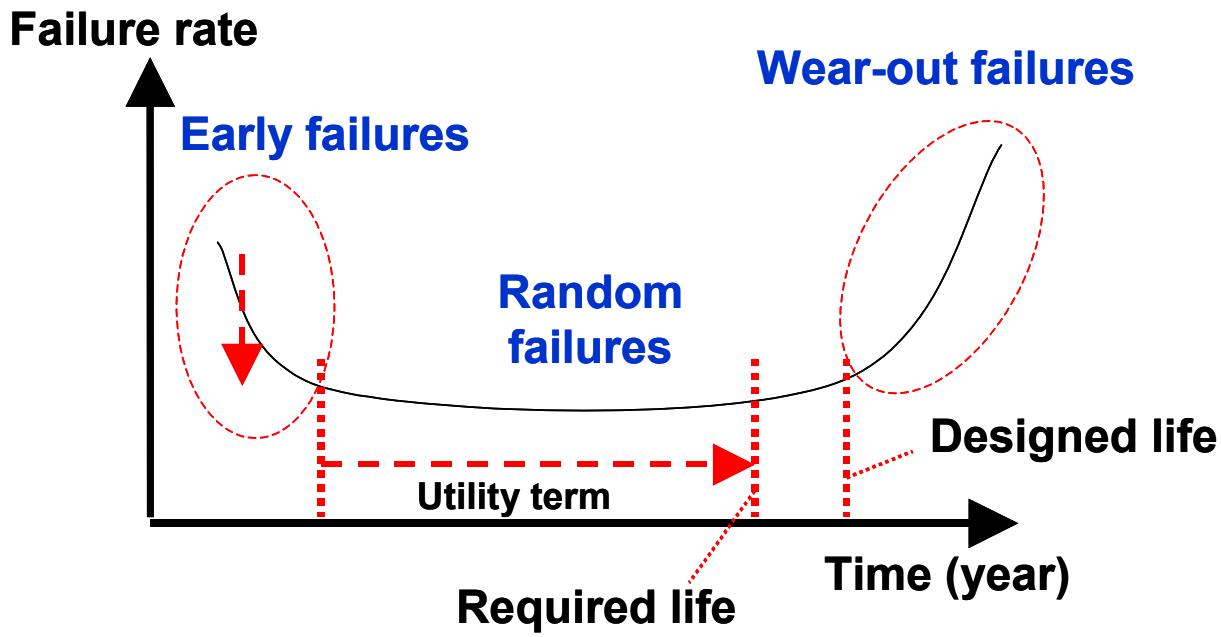
CONTENTS

Market of the power modules has widely been spread among the various applications, such as green energy conversion and electric vehicle in addition to conventionally used genera purpose inverter, servo, NC and elevator applications. Up to now, Fuji electric has tried to match the market demand for the power modules. In future, preferred properties for various applications are expected to have more varieties and/or higher functionality depending on the market growth. The reliability of power modules are getting more and more important to match these demands.

In this section, reliability for power modules, especially IGBT modules, will be described.

1 Basis of the reliability

In general, the time-dependent change in the failure rate of electronics parts and components including power modules is known as bathtub curve as shown in Fig.1. The curve can be comprised three parts of early failures, random failures and wear-out failures.



Early failures in IGBT modules would be caused by micros defects or human errors, which are originated defects in IGBTs and FWDs, cracking in DCBs, touch of gate and emitter wiring and so on.

Continuing the quality improvement activity can reduce such defects or errors. However, since complete removal of these inconveniences are very difficult, screening tests in out-going procedure are necessary to reject such early failures. Fuji Electric is continuing to prevent defective products leaving out from factory..

Failure rate of random failures coming after the early failures is relatively stable. Duration of random failure depends on operating conditions including environments of whole systems where IGBT modules and other components are installed. This means that failure rate of random failures is equivalent to the system-specific reliability. Therefore, random failures are in general caused by excessive stresses over maximum rating such as overvoltage, overcurrent, overheat and so on. The various reliability tests have been performed to decrease failure rates during random failure.

The unlikely failures during wear-out part are difficult to control procedures above because it is caused by wear or fatigue of the products.

It is important to select type of IGBT module to match the lifetime design in system taking into account of wear-out duration of IGBT module. Even though IGBT modules are fabricated on the well controlled production process, , the product lifetime not only depends on the operating conditions and/or environments, but also depends on how much design margin left in practical system.

2 Reliability test conditions

As described the previous section, the various reliability tests are performed to decrease failure rates of random failure, these tests are also for confirmation of new design.

Tables 1-1 and 1-2 show some parts of representative reliability test condition for the six-generation V-IGBTs. These conditions are governed by JEITA. Refer to the specification sheets in details.

Table 1-1 Reliability test condition (environment tests)

Test categories		Test items	Test methods and conditions	Reference norms EIAJ ED-4701 (Aug.-2001 edition)	Number of sample	Acceptance number
Environment Tests	1	High Temperature Storage	Storage temp. : 125±5 ℃ Test duration : 1000hr.	Test Method 201	5	(0 : 1)
	2	Low Temperature Storage	Storage temp. : -40±5 ℃ Test duration : 1000hr.	Test Method 202	5	(0 : 1)
	3	Temperature Humidity Storage	Storage temp. : 85±2 ℃ Relative humidity : 85±5% Test duration : 1000hr.	Test Method 103 Test code C	5	(0 : 1)
	4	Unsaturated Pressurized Vapor	Test temp. : 120±2 ℃ Test humidity : 85±5% Test duration : 96hr.	Test Method 103 Test code E	5	(0 : 1)
	5	Temperature Cycle	Test temp. : Low temp. -40±5 ℃ High temp. 125 ±5 ℃ RT 5 ~ 35 ℃ Dwell time : High ~ RT ~ Low ~ RT 1hr. 0.5hr. 1hr. 0.5hr. Number of cycles : 100 cycles	Test Method 105	5	(0 : 1)
	6	Thermal Shock	Test temp. : High temp. 100^{+0}_{-5} ℃ Low temp. 0^{+5}_{-0} ℃ Used liquid : Water with ice and boiling water Dipping time : 5 min. par each temp. Transfer time : 10 sec. Number of cycles : 10 cycles	Test Method 307 method Ⅰ Condition code A	5	(0 : 1)

Table 1-2 Reliability test condition (endurance tests)

Test categories		Test items	Test methods and conditions	Reference norms EIAJ ED-4701 (Aug.-2001 edition)	Number of sample	Acceptance number
Endurance Tests	1	High temperature Reverse Bias	Test temp. : Tj = 150°C (-0 °C/+5 °C) Bias Voltage : VC = 0.8×VCES Bias Method : Applied DC voltage to C-E VGE = 0V Test duration : 1000hr.	Test Method 101	5	(0 : 1)
	2	High temperature Bias (for gate)	Test temp. : Tj = 150°C (-0 °C/+5 °C) Bias Voltage : VC = VGE = +20V or -20V Bias Method : Applied DC voltage to G-E VCE = 0V Test duration : 1000hr.	Test Method 101	5	(0 : 1)
	3	Temperature Humidity Bias	Test temp. : 85±2 °C Relative humidity : 85±5% Bias Voltage : VC = 0.8×VCES Bias Method : ; voltage to C-E VGE = 0V Test duration : 1000hr.	Test Method 102 Condition code C	5	(0 : 1)
	4	Intermitted Operating Life (Power cycle) (for IGBT)	ON time : 2 sec. OFF time : 18 sec. Test temp. : 100±5 deg Tj ≦ 150 °C, Ta=25±5 °C Number of cycles : 15000 cycles	Test Method 106	5	(0 : 1)

As shown in table 1-2, it should be noted that high temperature reverse bias and high temperature bias to gate are done at junction temperature of 150°C in order to guarantee 150°C continuous operation.

3 Power cycle curve

The IGBT module has temperature swing depending on its operating conditions. The mechanical stress in each internal structure of the IGBT module will be accumulated over thermal stress and then it results mechanical fatigue and deterioration. This fatigue and deterioration strongly depend on the amount of temperature swing of up and down and it also limits the IGBT product lifetime depending on the operating and environmental conditions. This type of temperature cycle is typically called as "power cycle life (power cycle capability)". The power cycle life can be estimated from the power cycle capability curves indicating the relation between the temperature swing ΔT and the number of cycles. There are two types of curves are practically important for system design.

One is the ΔTj power cycle (ΔTj-P/C) capability curves, which are the life curves made when the junction temperature rapid rises and falls. In these curves, failure caused by deterioration at the interface between the aluminum bonding wire and chip surface interconnection. The other is the ΔTc power cycle (ΔTc-P/C) capability curves, which predict the product lifetime curve which is limited by the change in the case temperature (mainly the base plate temperature). In this case, a predominant failure caused by deterioration of the soldered joints between the insulated substrate DCB and the copper base plate.

The following sections describe the measurement method and the power cycle capability curves for the ΔTj-P/C and ΔTc-P/C power cycles, respectively.

3.1 ΔTj power cycle (ΔTj-P/C) capability curves

Figure 11-2 shows the patterns of current flow in the ΔTj power cycle (ΔTj-P/C) test. Figures 11-3 and 11-4 show the equivalent schematic circuit in the ΔTj power cycle test and the schematic view of the Tc and Tf measurement positions, respectively. During the ΔTj power cycle test, the junction temperature goes up and down in a short-time cycle. Therefore, outstanding temperature difference between silicon chip and DCB or bonding wires results thermal stress. For this reason, the ΔTj power cycle lifetime is mainly limited by the aluminum bonding wire joints and the soldered layer under the chip.

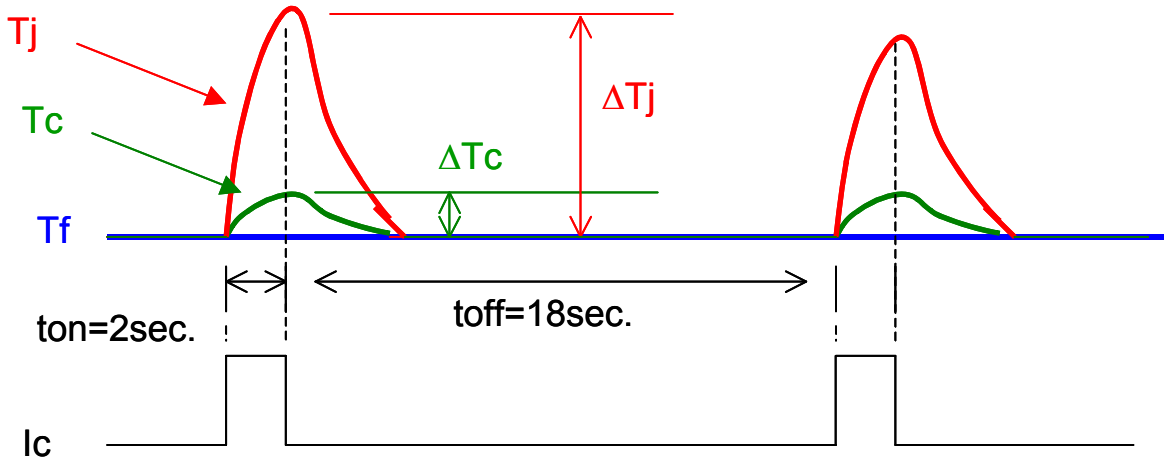


Fig. 11-2 Pattern diagram of current flow of ΔTj power cycle and temperature change

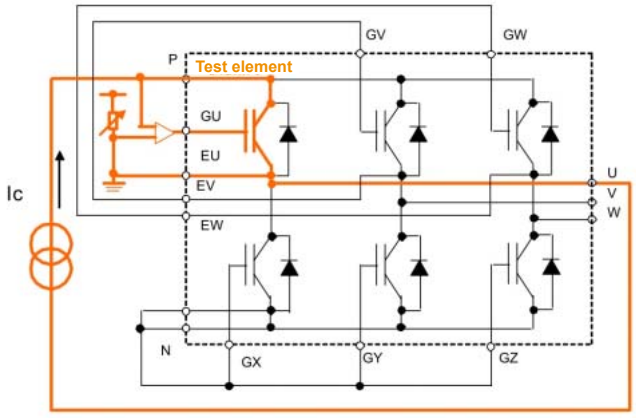


Fig. 11-3 Equivalent circuit for ΔTj power cycle test

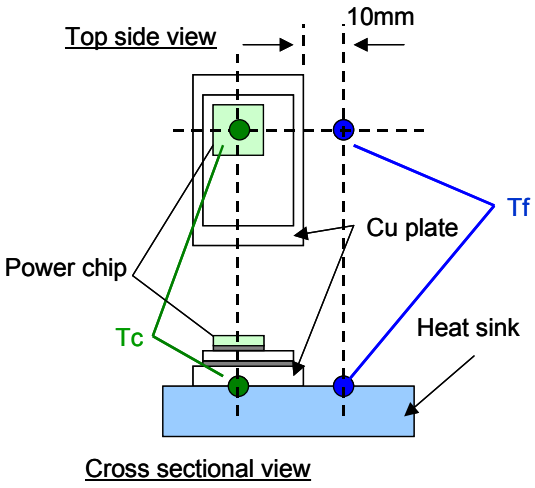


Fig. 11-4 Schematic view of Tc and Tf measurement positions

Figure 11-5 shows the curves of U series and V series as an example of ΔTj power cycle capability curve of the IGBT module. In this figure, the Tjmin=25°C line indicates the life cycle of fixed minimum temperature. The chip temperature is changed while the temperature of the cooling fin is kept at 25°C. For example, when ΔTj = 50°C, the chip temperature reaches 75°C while the cooling fin temperature is 25°C. On the other hand, the Tjmax=150°C line shows the life cycle of fixed maximum temperature. The temperature of cooling fin is changed but the maximum junction temperature of the chip is fixed to 150°C. For example, when ΔTj = 50°C, the chip maximum junction temperature is 150°C while the temperature of the cooling fin is 100°C. As shown in the figure, even at the same ΔTj, the higher the temperature of the cooling fin and the achieving temperature of the

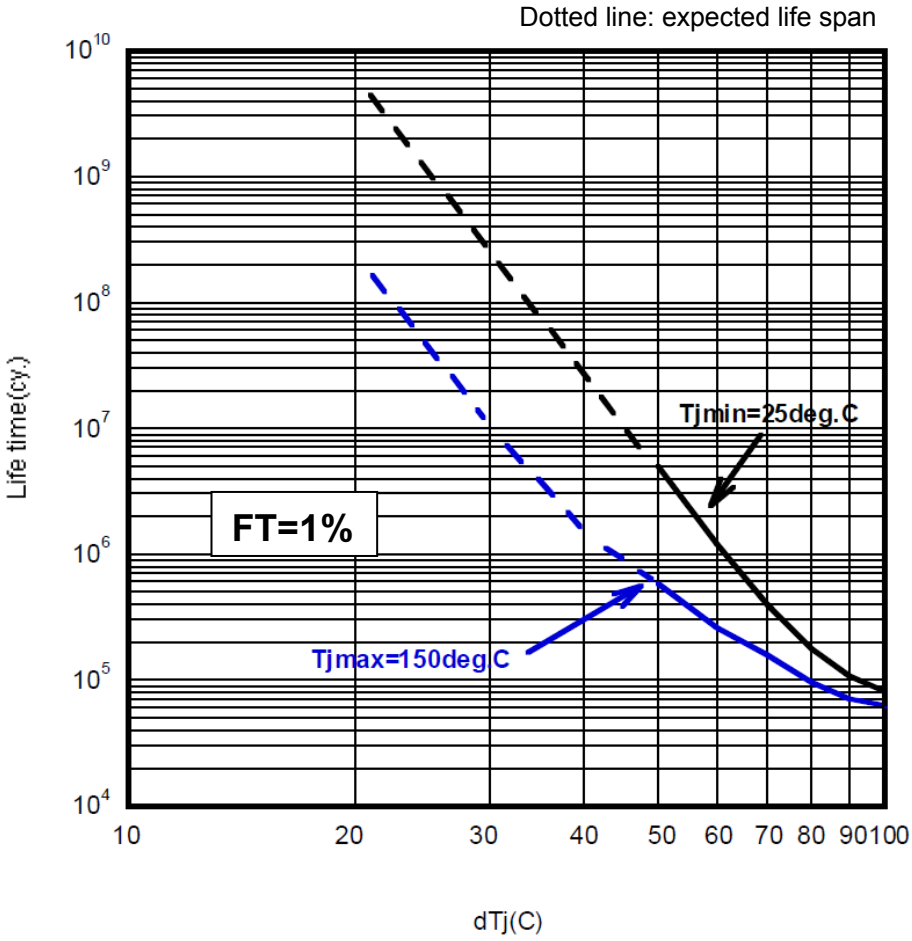


Fig. 11-5 Example of ΔTj power cycle capability curve (F(t) = 1% Chips connected in parallel are excluded. The dotted lines indicate the expected life span.)

chip are, the shorter the estimated life span will be.

For safe life design of the IGBT module in practical system, it is important to check ΔTj in various operating conditions of the equipment to make sure the power cycle life with the chart provided above so that the IGBT expected product lifetime has longer enough than the specific life span of the product.

It should be noted that for the system, which have frequent acceleration/deceleration or frequent system start/stop such as Fig 11-6 as one of examples, should be careful in reliability lifetime prediction.

In such equipment, ΔTj should be defined as the difference between the maximum junction temperature Tj and the fin temperature Tf (see Figure 11-2), and then make sure that its life is longer enough than the targeted life span of the product. It is important for such system not to use parameters in steady-state. Because the product lifetime is limited by much higher temperature swing at acceleration/deceleration or start/stop compared to the steady state.

In addition, drive systems which run low speed operation such as 0.5Hz output should have similar notice since the temperature swing at low speed operation may have much higher than steady-state.

If there are multiple load profile of acceleration, deceleration and/or low-speed operation temperatures within one operation cycle of the equipment, calculate the power cycle life according to the “Calculation of life span when there are multiple temperature rises” described later.

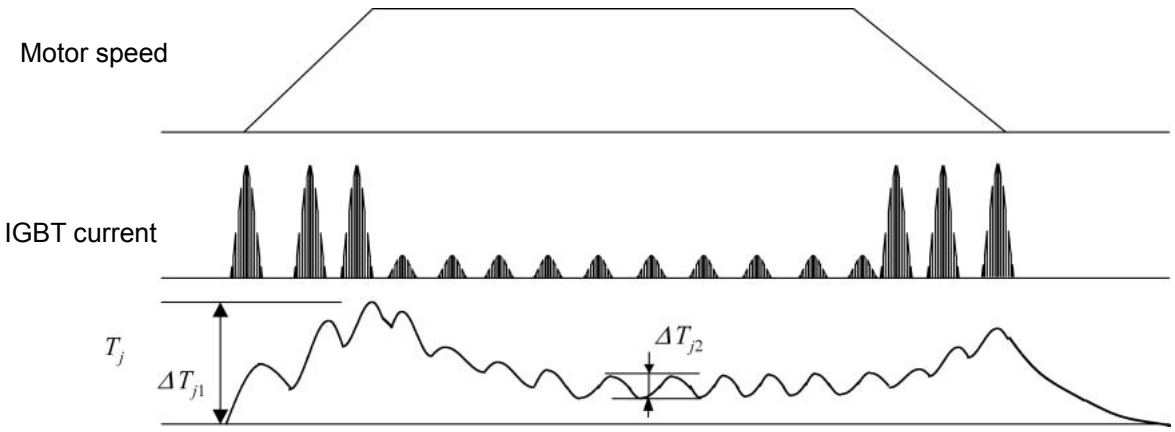


Fig. 11-6 Operation in actual inverter (example)

3.2 ΔTc power cycle (ΔTc-P/C) capability curve

Figure 11-7 shows the current flow pattern of ΔTc power cycle (ΔTc-P/C) in Fuji IGBT reliability test. Figure 11-8 shows the equivalent schematic circuit in the ΔTc power cycle test for the 6in1 module. During the ΔTc power cycle test, all switches (6 switches in the 6in1 module, and 2 switches in the 2in1 module) are electrically active state, and the temperature of the entire case (mainly the copper base) can be controlled to increased and decreased. However, the case temperature Tc is increased and decreased in a relatively long-time cycle so that the difference between the junction temperature Tj and the case temperature Tc becomes small. This is different from the conditions in the ΔTj power cycle test. When such temperature change occurs, the significant stress strain becomes predominant between the base and the insulated substrate DCB. The power cycle of this operation mode is limited by the soldered joints under the insulated substrate DCB.

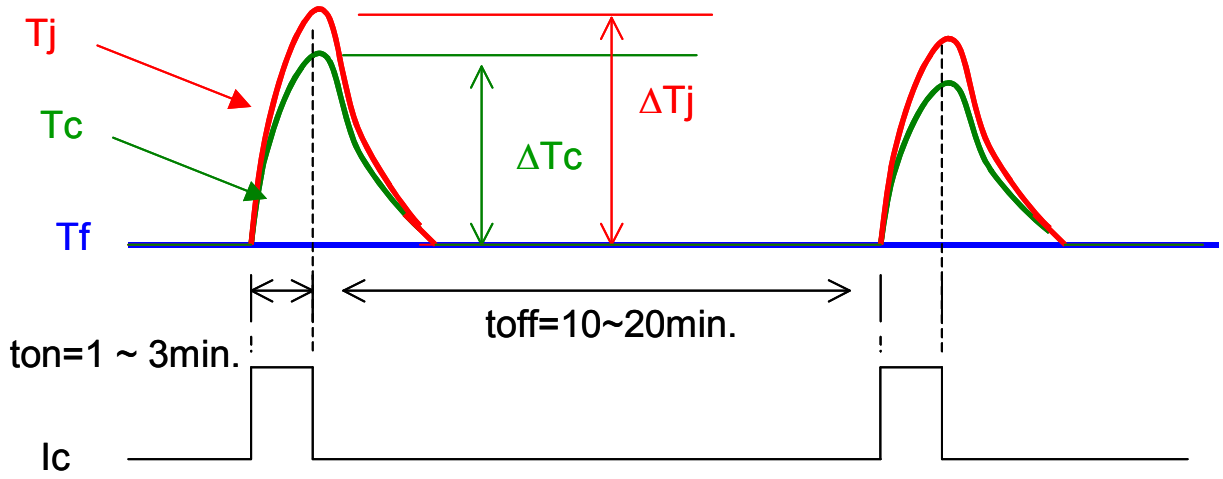


Fig. 11-7 Current flow pattern of ΔTc power cycle

The failure mode of the ΔTc power cycle can be explained as follows. When the case temperature Tc is increased and decreased, the largest stress strain is caused in the soldered joint between the insulated substrate DCB and the base due to the difference in thermal expansion coefficient between them. When this heat change is repeated, the soldered joint is cracked due to the stress strain. When this crack advances up to the lower part of the insulated substrate DCB, on which the silicon chip is installed, the chip junction temperature Tj rises because the heat radiation of the silicon chip is deteriorated (the thermal resistance Rth increases). As a result, the chip junction temperature Tj may exceed Tjmax and thermal destruction may result.

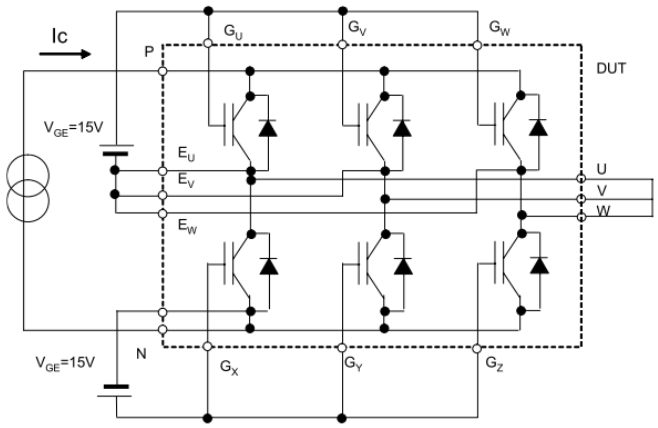


Fig. 11-8 Equivalent circuit for ΔTc power cycle test

Figure 11-9 shows the ΔTc power cycle curve in the IGBT module. When the temperature difference between the joint and the case is small and the temperature of the case rises and falls repeatedly, make sure in design that the operation life of the module, which is obtained from the ΔTc power cycle curve, is longer enough than the targeted design life of the product.

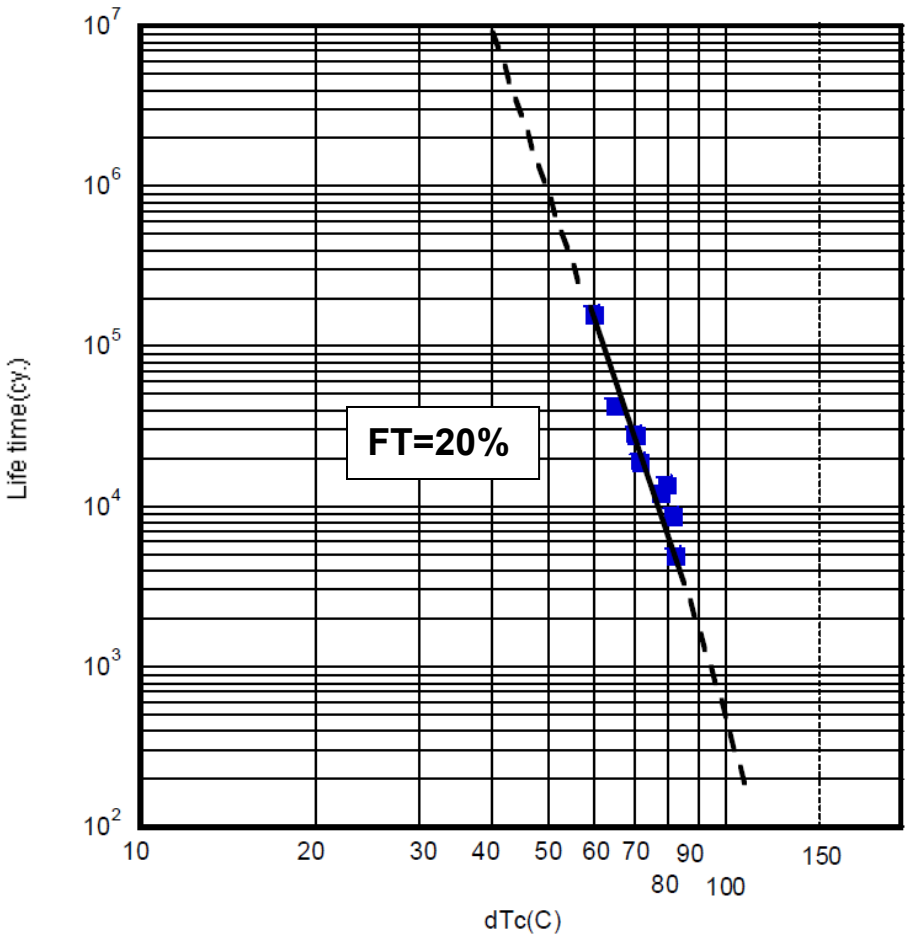


Fig. 11-9 Example of ΔTc power cycle capability

(DCB substrate: Al_2O_3 / lower part of DCB soldered: Sn type lead-free solder)

3.3 Calculation of power cycle life when there are multiple temperature rises in one operation cycle of equipment

The power cycle life of the IGBT module depends on height the temperature swing (and the maximum temperature) during power cycle. Therefore, when there is only one temperature rise peak of the IGBT module in one operation cycle of the inverter, the number of times calculated from the power cycle life curve is the life cycle of the IGBT module.

However, when there are multiple temperature rise peaks in one operation cycle of the inverter, the life cycle becomes shorter because the module is influenced by the multiple temperature rises. The calculation method of power cycle life when there are multiple different temperature rise peaks is shown below.

When there are n times of temperature rises in one operation cycle of inverter, the combined power cycle life can be expressed in the following formula, where PC(k) is the power cycle life for the k-th (k=1, 2, 3, …., n) temperature rise.

$$PC = 1/\left(\sum_{k=1}^{n}\frac{1}{PC(k)}\right)$$

For example, when n=4 and the power cycle numbers for the respective power rise peaks are 3.8 x 10^6, 1.2 x 10^6, 7.6 x 10^5 and 4.6 x 10^5, calculation is made as follows:

$$PC = 1/\left(\frac{1}{3.8\,\mathrm{x}10^6}+\frac{1}{1.2\,\mathrm{x}10^6}+\frac{1}{7.6\,\mathrm{x}10^5}+\frac{1}{4.6\,\mathrm{x}10^5}\right) = 2.2\,\mathrm{x}10^5$$

Therefore, the power cycle lifetime can be obtained from the product of the power cycle life calculated in this way and one cycle (time) of operation mode.

For example, when one cycle of the above operation mode is 1800sec (30min), the lifetime is calculated as follows:

2.2 x 10^5 x 1800 / (60 x 60 x 24 x 365) = 12.55 ≈12 years and 6 months.

WARNING

1. This Catalog contains the product specifications, characteristics, data, materials, and structures as of May 2011.
The contents are subject to change without notice for specification changes or other reasons. When using a product listed in this Catalog, be sur to obtain the latest specifications.

2. All applications described in this Catalog exemplify the use of Fuji's products for your reference only. No right or license, either express or implied, under any patent, copyright, trade secret or other intellectual property right owned by Fuji Electric Co., Ltd. is (or shall be deemed) granted. Fuji Electric Co., Ltd. makes no representation or warranty, whether express or implied, relating to the infringement or alleged infringement of other's intellectual property rights which may arise from the use of the applications described herein.

3. Although Fuji Electric Co., Ltd. is enhancing product quality and reliability, a small percentage of semiconductor products may become faulty. When using Fuji Electric semiconductor products in your equipment, you are requested to take adequate safety measures to prevent the equipment from causing a physical injury, fire, or other problem if any of the products become faulty. It is recommended to make your design failsafe, flame retardant, and free of malfunction.

4. The products introduced in this Catalog are intended for use in the following electronic and electrical equipment which has normal reliability requirements.
- Computers
- OA equipment
- Communications equipment (terminal devices)
- Measurement equipment
- Machine tools
- Audiovisual equipment
- Electrical home appliances
- Personal equipment
- Industrial robots etc.

5. If you need to use a product in this Catalog for equipment requiring higher reliability than normal, such as for the equipment listed below, it is imperative to contact Fuji Electric Co., Ltd. to obtain prior approval. When using these products for such equipment, take adequate measures such as a backup system to prevent the equipment from malfunctioning even if a Fuji's product incorporated in the equipment becomes faulty.
- Transportation equipment (mounted on cars and ships)
- Trunk communications equipment
- Traffic-signal control equipment
- Gas leakage detectors with an auto-shut-off feature
- Emergency equipment for responding to disasters and anti-burglary devices
- Safety devices
- Medical equipment

6. Do not use products in this Catalog for the equipment requiring strict reliability such as the following and equivalents to strategic equipment (without limitation).
- Space equipment
- Aeronautic equipment
- Nuclear control equipment
- Submarine repeater equipment

8. If you have any question about any portion in this Catalog, ask Fuji Electric Co., Ltd. or its sales agents before using the product.
Neither Fuji Electric Co., Ltd. nor its agents shall be liable for any injury caused by any use of the products not in accordance with instructions set forth herein.